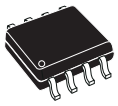
TS922, TS922A

Datasheet

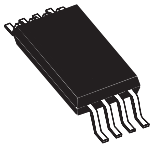
Rail-to-rail, high output current, dual operational amplifier



Flip-chip with backcoating



SO8



TSSOP8

Product status link
TS922 and TS922A

Features

- Rail-to-rail input and output
- Low noise: 9 nV/√Hz
- Low distortion
- High output current: 80 mA (able to drive 32 Ω loads)
- High-speed: 4 MHz, 1 V/µs
- Operating from 2.7 to 12 V
- Low input offset voltage: 900 µV max. (TS922A)
- ESD internal protection: 2 kV
- Latch-up immunity

Applications

- Line drivers and actuator drivers
- Portable speakers
- Instrumentation with low noise as key factor
- Multimedia systems and portable equipments

Description

The TS922 and the TS922A devices are rail-to-rail dual BiCMOS operational amplifiers optimized and fully specified for 3 V and 5 V operations. These devices have high output currents which allow low-load impedances to be driven.

Very low noise, low distortion, low offset, and a high output current capability make these devices an excellent choice for high quality, low voltage, or battery operated audio systems.

The devices are stable for capacitive loads up to 500 pF.

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1 Pin diagrams

Figure 1. Pinout for Flip-chip package (top view)

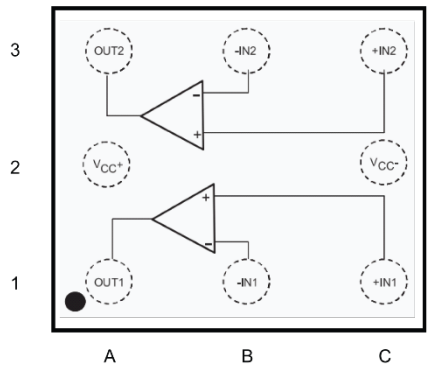
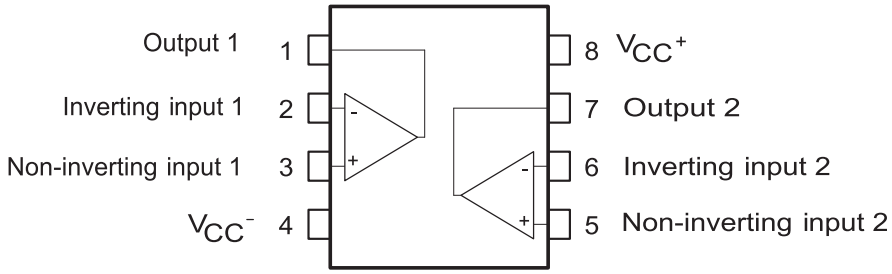


Figure 2. Pin connections for SO8 and TSSOP8 (top view)



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2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		14	V
V_{id}	Differential input voltage (2)		±1	
V_{in}	Input voltage (3)		(V_{CC-}) - 0.3 to (V_{CC+}) + 0.3	
T_{stg}	Storage temperature		-65 to 150	°C
T_j	Maximum junction temperature		150	
—	Soldering temperature (10 s), leaded version		250	
—	Soldering temperature (10 s), unleaded version		260	
R_{thja}	Thermal resistance junction-to-ambient (4)	Flip-chip	90	°C/W
		SO8	125	
		TSSOP8	120	
R_{thjc}	Thermal resistance junction-to-case (4)	SO8	40	
		TSSOP8	37	
ESD	HBM: human body model (5)		2000	V
	MM: machine model (6)		120	
	CDM: charged device model (7)		1500	
—	Latch-up immunity		200	mA
—	Output short-circuit duration		See note (8)	

1. *All voltage values, except the differential voltage are with respect to network ground terminal.*
2. *The differential voltage is the non-inverting input terminal with respect to the inverting input terminal. If V_{id} > ±1 V, the maximum input current must not exceed ±1 mA. In this case (V_{id} > ±1 V), an input series resistor must be added to limit the input current.*
3. *Do not exceed 14 V.*
4. *Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers. These values are typical.*
5. *Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.*
6. *Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of pin combinations with other pins floating.*
7. *Charged device model: all pins and plus package are charged together to the specified voltage and then discharged directly to ground.*
8. *There is no short-circuit protection inside the device: short-circuits from the output to V_{CC} can cause excessive heating. The maximum output current is approximately 80 mA, independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.*

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 12	V
V_{icm}	Common mode input voltage range	(V_{CC-}) - 0.2 to (V_{CC+}) + 0.2	
T_{oper}	Operating free air temperature range	-40 to 125	°C

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3 Electrical characteristics

Table 3. Electrical characteristics measured at V_{CC} = 3 V, V_{CC}- = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	TS922			3	mV
		TS922A			0.9	
		TS922EIJT			1.5	
		$T_{min} \le T_{amb} \le T_{max}$, TS922			5	
		$T_{min} \le T_{amb} \le T_{max}$, TS922A			1.8	
		$T_{min} \le T_{amb} \le T_{max}$, TS922EIJT			2.5	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current	$V_{out} = V_{CC}/2$		1	30	nA
		$T_{min} \le T_{amb} \le T_{max}$			30	
I_{ib}	Input bias current	$V_{out} = V_{CC}/2$		15	100	
		$T_{min} \le T_{amb} \le T_{max}$			100	
V_{OH}	High level output voltage	R_L= 10 kΩ	2.90			V
		$T_{min} \le T_{amb} \le T_{max}$	2.90			
		R_L = 600 Ω	2.87			
		$T_{min} \le T_{amb} \le T_{max}$	2.87			
		R_L = 32 Ω		2.63		
V_{OL}	Low level output voltage	R_L= 10 kΩ			50	mV
		$T_{min} \le T_{amb} \le T_{max}$			50	
		R_L = 600 Ω			100	
		$T_{min} \le T_{amb} \le T_{max}$			100	
		R_L = 32 Ω		180		
A_{vd}	Large signal voltage gain	R_L= 10 kΩ, V_{out} = 2 V_{p-p}		200		V/mV
		$T_{min} \le T_{amb} \le T_{max}$	70			
		R_L = 600 Ω, V_{out} = 2 V_{p-p}		35		
		$T_{min} \le T_{amb} \le T_{max}$	15			
		R_L = 32 Ω, V_{out} = 2 V_{p-p}		16		
I_{CC}	Total supply current	No load, $V_{out} = V_{CC}/2$		2	3	mA
		$T_{min} \le T_{amb} \le T_{max}$			3.2	
GBP	Gain bandwidth product	R_L = 600 Ω		4		MHz
CMR	Common mode rejection ratio	V_{icm} = 0 to 3 V	60	80		dB
		$T_{min} \le T_{amb} \le T_{max}$	56			
SVR	Supply voltage rejection ratio	V_{CC} = 2.7 to 3.3 V	60	85		dB
		$T_{min} \le T_{amb} \le T_{max}$	60			
I_o	Output short-circuit current		50	80		mA

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Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SR	Slew rate		0.7	1.3		V/µs
ϕm	Phase margin at unit gain	R_L = 600 Ω, C_L = 100 pF		68		Degrees
G_m	Gain margin	R_L = 600 Ω, C_L = 100 pF		12		dB
e_n	Equivalent input noise voltage	f = 1 kHz		9		nV/√Hz
THD	Total harmonic distortion	V_{out} = 2 V_{p-p}, f = 1 kHz, A_v = 1, R_L = 600 Ω		0.005		%
C_s	Channel separation			120		dB

Table 4. Electrical characteristics measured at V_{CC} = 5 V, V_{CC}- = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	TS922			3	mV
		TS922A			0.9	
		TS922EIJT			1.5	
		T_{min} ≤ T_{amb} ≤ T_{max}, TS922			5	
		T_{min} ≤ T_{amb} ≤ T_{max}, TS922A			1.8	
		T_{min} ≤ T_{amb} ≤ T_{max}, TS922EIJT			2.5	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current	V_{out} = V_{CC}/2		1	30	nA
		T_{min} ≤ T_{amb} ≤ T_{max}			30	
I_{ib}	Input bias current	V_{out} = V_{CC}/2		15	100	
		T_{min} ≤ T_{amb} ≤ T_{max}			100	
V_{OH}	High level output voltage	R_L= 10 kΩ	4.9			V
		T_{min} ≤ T_{amb} ≤ T_{max}	4.9			
		R_L = 600 Ω	4.85			
		T_{min} ≤ T_{amb} ≤ T_{max}	4.85			
		R_L = 32 Ω		4.4		
V_{OL}	Low level output voltage	R_L= 10 kΩ			50	mV
		T_{min} ≤ T_{amb} ≤ T_{max}			50	
		R_L = 600 Ω			120	
		T_{min} ≤ T_{amb} ≤ T_{max}			120	
		R_L = 32 Ω		300		
A_{vd}	Large signal voltage gain	R_L= 10 kΩ, V_{out} = 2 V_{p-p}		200		V/mV
		T_{min} ≤ T_{amb} ≤ T_{max}	70			
		R_L = 600 Ω, V_{out} = 2 V_{p-p}		35		
		T_{min} ≤ T_{amb} ≤ T_{max}	20			
		R_L = 32 Ω, V_{out} = 2 V_{p-p}		16		
I_{cc}	Total supply current	No load, V_{out} = V_{CC}/2		2	3	mA
		T_{min} ≤ T_{amb} ≤ T_{max}			3.2	

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
GBP	Gain bandwidth product	R_L = 600 Ω		4		MHz
CMR	Common mode rejection ratio	V_{icm} = 0 to 5 V	60	80		dB
		$T_{min} \leq T_{amb} \leq T_{max}$	56			
SVR	Supply voltage rejection ratio	V_{CC} = 4.5 to 5.5 V	60	85		
		$T_{min} \leq T_{amb} \leq T_{max}$	60			
I_o	Output short-circuit current		50	80		mA
SR	Slew rate		0.7	1.3		V/µs
ϕm	Phase margin at unit gain	R_L = 600 Ω, C_L =100 pF		68		Degrees
G_m	Gain margin			12		dB
e_n	Equivalent input noise voltage	f = 1 kHz		9		nV/√Hz
THD	Total harmonic distortion	V_{out} = 2 V_{p-p}, f = 1 kHz, A_v = 1, R_L = 600 Ω		0.005		%
C_s	Channel separation			120		dB

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4 Electrical characteristic curves

Figure 3. Output short-circuit current vs. output voltage

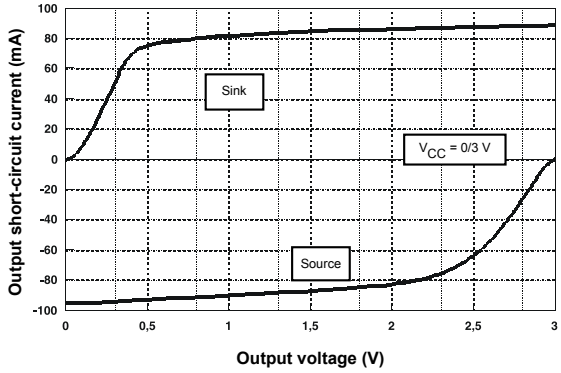


Figure 4. Total supply current vs. supply voltage

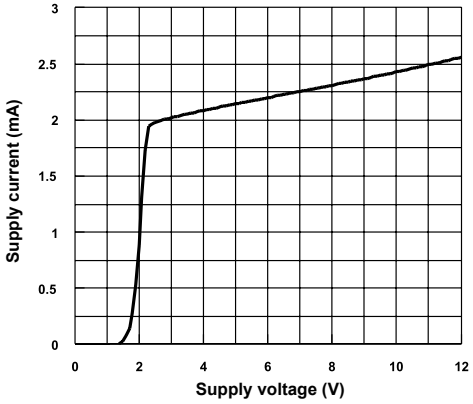


Figure 5. Voltage gain and phase vs. frequency

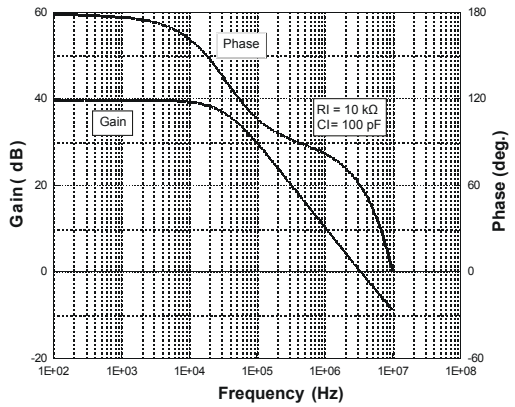


Figure 6. Equivalent input noise voltage vs. frequency

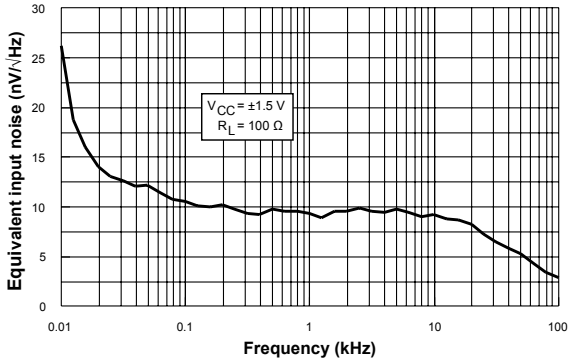


Figure 7. THD + noise vs. frequency (R_L = 2 kΩ, V_o = 10 Vpp, V_{CC} = ± 6 V)

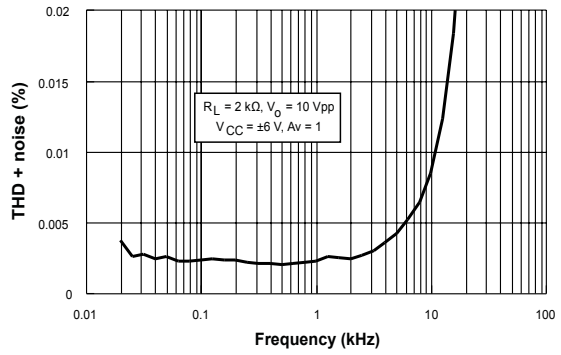
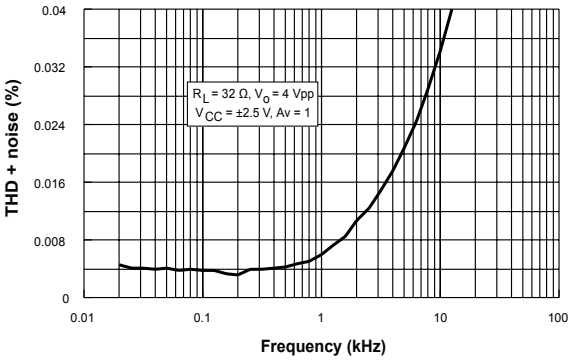


Figure 8. THD + noise vs. frequency (R_L = 32 Ω, V_o = 4 Vpp, V_{CC} = ± 2.5 V)



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Figure 9. THD + noise vs. frequency (R_L = 32 Ω, V_o = 2 Vpp, V_{CC} = ± 1.5 V)

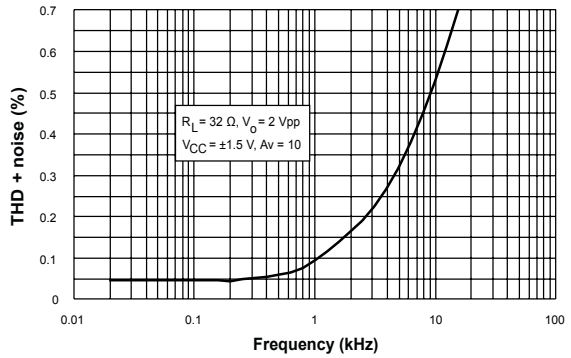


Figure 10. THD + noise vs. output voltage (R_L = 600 Ω, f = 1 kHz, V_{CC} = 0/3 V)

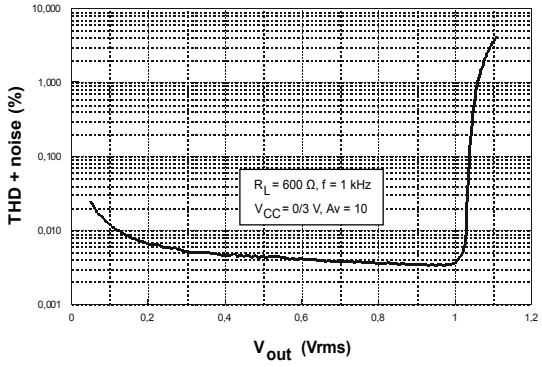


Figure 11. THD + noise vs. output voltage (R_L = 32 Ω, f = 1 kHz, V_{CC} = ± 1.5 V)

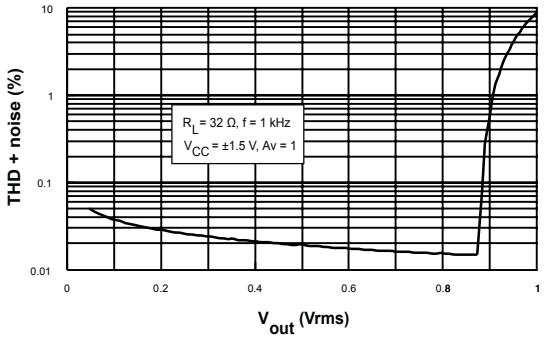


Figure 12. THD + noise vs. output voltage (R_L = 2 kΩ, f = 1 kHz, V_{CC} = ± 1.5 V)

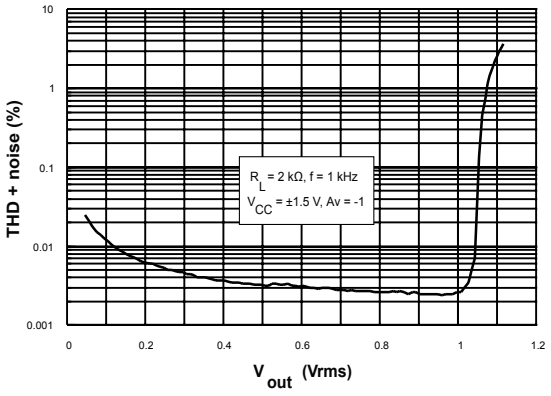
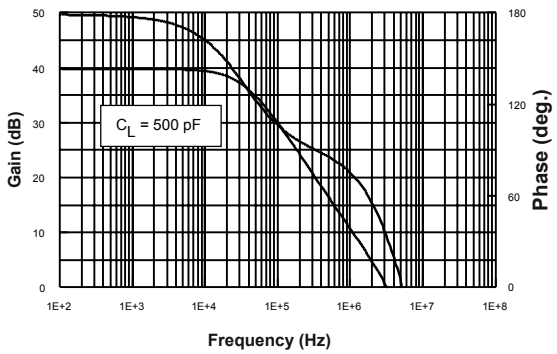


Figure 13. Open loop gain and phase vs. frequency



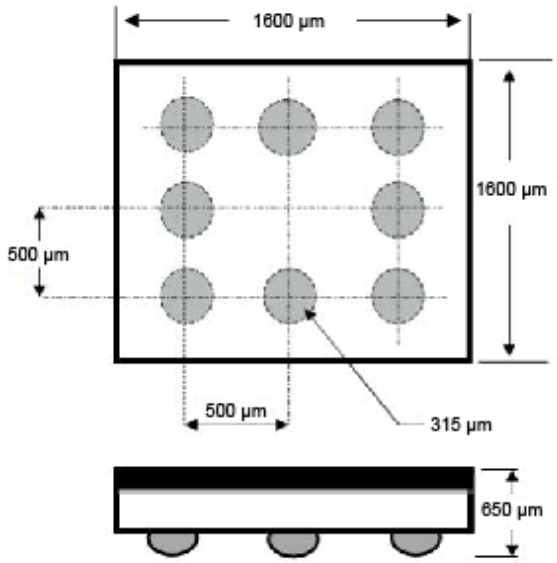
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5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 8-bump Flip-chip package information

Figure 14. 8-bump Flip-chip package dimensions (top view)



1. Die size: 1600 µm x 1600 µm ±30 µm, Die height: 350 µm ±20 µm, die height (including bumps): 650 µm, bump diameter: 315 µm ±50 µm, bump height: 250 µm ±40 µm, pitch: 500 µm ±10 µm, backcoating.

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Figure 15. **8-bump Flip-chip recommended footprint (TS922EIJT)**

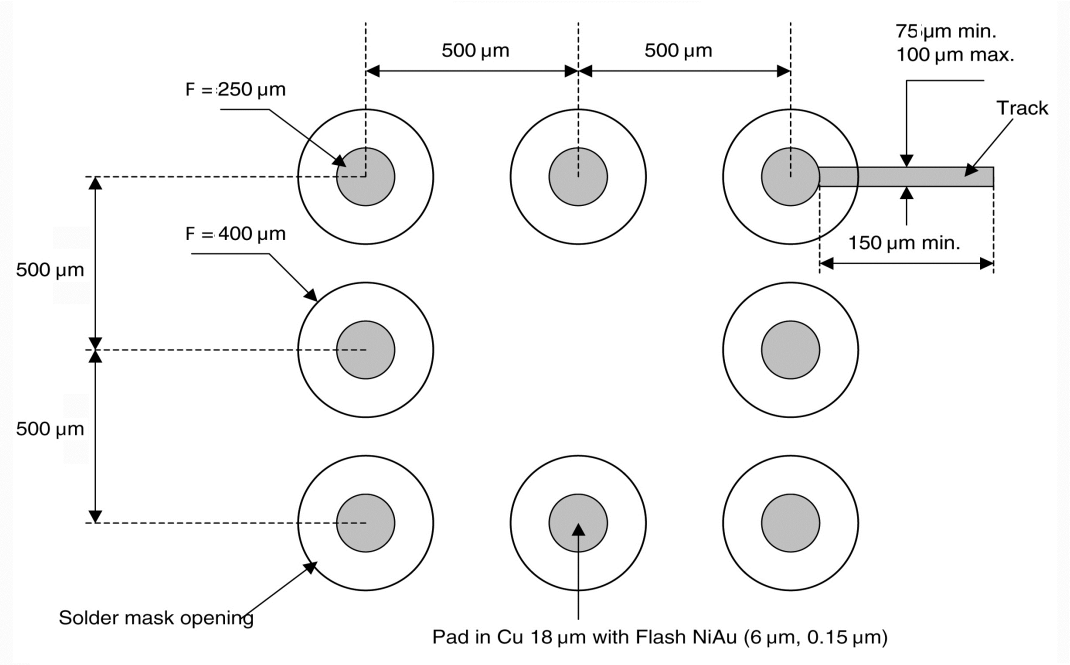
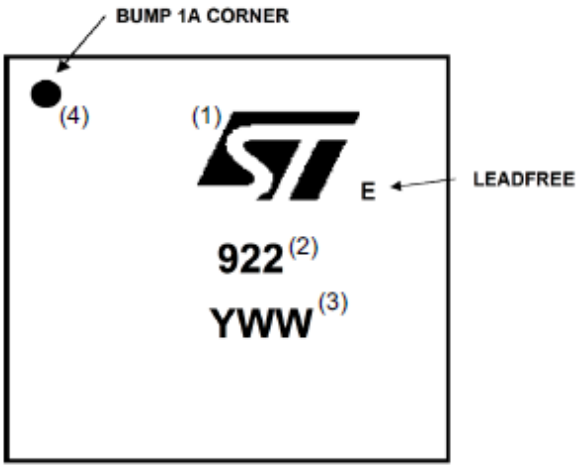


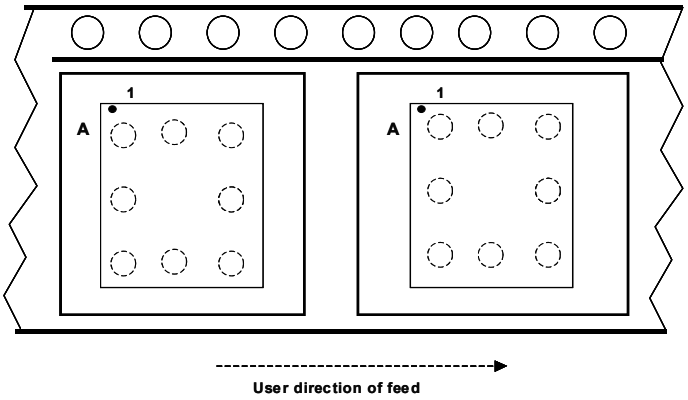
Figure 16. **8-bump Flip-chip marking (top view)**



1. ST logo
2. Part number
3. Date code: Y = year, WW = week
4. This dot indicates the bump corner 1A

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Figure 17. **8-bump Flip-chip tape and reel specification (top view)**



1. Device orientation: the devices are oriented in the carrier pocket with bump number A1 adjacent to the pocket holes.

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5.2 SO8 package information

Figure 18. **SO8 package outline**

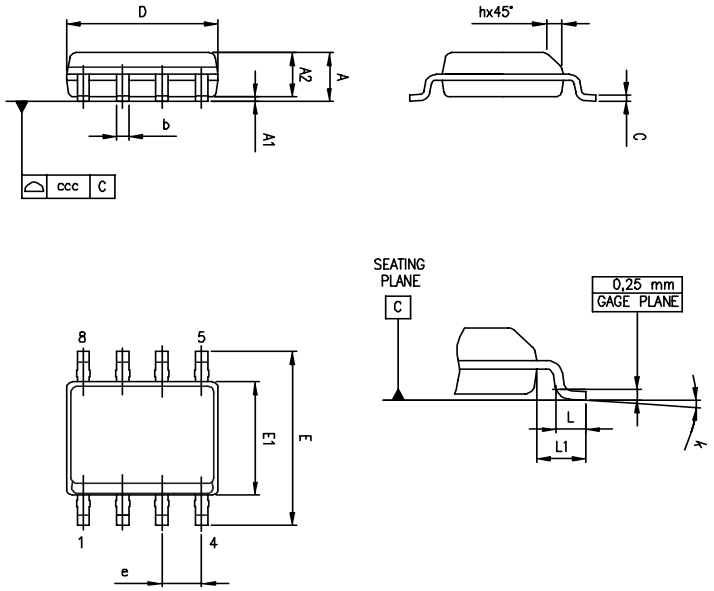


Table 5. **SO8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

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5.3 TSSOP8 package information

Figure 19. **TSSOP8 package outline**

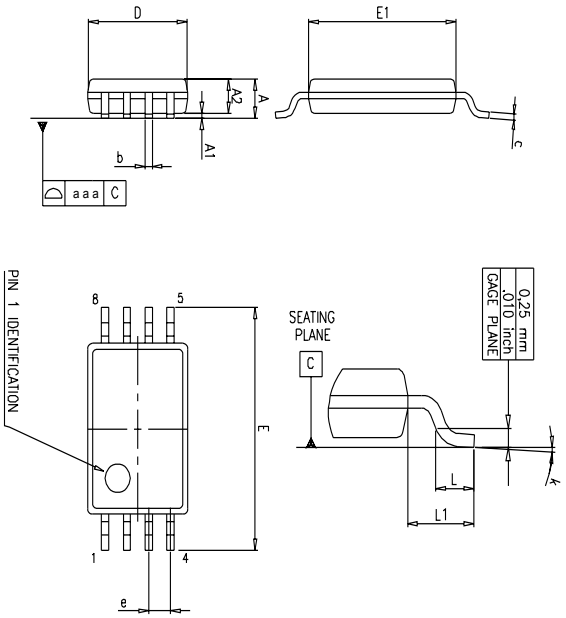


Table 6. **TSSOP8 mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.1			0.004	

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6 Ordering information

Table 7. Ordering information

Order code	Temperature range	Package	Packing	Marking
TS922ID	-40 °C to 125 °C	SO8	Tube or tape and reel	922I
TS922IDT				
TS922AID				922AI
TS922AIDT				
TS922IYDT (1)		SO8 (automotive grade)		922IY
TS922AIYDT (1)			Tape and reel	922AIY
TS922IPT		TSSOP8		922I
TS922AIPT				922AI
TS922IYPT (1)		TSSOP8 (automotive grade)		922IY
TS922AIYPT (1)				922AY
TS922EIJT		Flip-chip with backcoating		922

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent.*

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Revision history

Table 8. **Document revision history**

Date	Revision	Changes
01-Feb-2001	1	First release.
01-Jul-2004	2	Flip-chip package inserted in the document.
02-May-2005	3	Modifications in AMR Table 1 (explanation of V_{id} and V_i limits, ESD MM and CDM values added, R_{thja} added).
01-Aug-2005	4	PPAP references inserted in the datasheet, see Table 8.
01-Mar-2006	5	TS922EIJT part number inserted in the datasheet, see Table 8.
26-Jan-2007	6	Modifications in AMR Table 1 (R_{thjc} added), parameter limits on full temperature range added in Table 3 and Table 4.
12-Nov-2007	7	Added notes on ESD in AMR table. Re-formatted package information. Added notes for automotive grade in order codes table.
02-Feb-2010	8	Document reformatted. Added root part number TS922A on cover page. Removed TS922AIYD order code from Table 8.
15-Jan-2013	9	Added MiniSO8 package. Modified test conditions for CMR in Table 3 and Table 4. Replaced V_{DD} by V_{CC-} in title of Table 3, Table 4, and Table 5. Updated titles of Figure 7 to Figure 12 (added conditions to differentiate them). Removed TS922IYD device from Table 8. Minor corrections throughout document.
04-Jun-2013	10	Features: updated package information for Flip-chip Figure 2: Updated title Table 1: updated footnotes 5, 6, and 7 Table 3 and Table 4: replaced DVio with ΔVio/ΔT Figure 14: added backcoating to package information Figure 16: updated footnote 3 Table 8: updated package information for Flip-chip
27-Jun-2013	11	Figure 14: updated to include new height for backcoating
20-Jan-2016	12	Updated document layout Removed MiniSO8 and DIP8 packages Updated cover image: removed J, D (plastic micropackage), and P (thin shrink small outline package) respectively from Flip-chip with backcoating, SO8, and TSSOP packages. Table 6: updated SO8 information for min “k” parameter (mm dimensions) Table 7: updated “aaa” information. These are “typ” not "max" values. Table 8: "Order codes": removed following order codes: TS922IST, TS922AIST, TS922IN, TS922IYST. TS922AIYST, and TS922IJT.

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Date	Revision	Changes
20-Jul-2018	13	Updated features and applications in cover page. Updated Figure 1. Pinout for Flip-chip package (top view). Updated Section 6 Ordering information. Removed "Macromodel" section. Minor text changes.

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