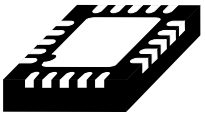
PM8908

Monolithic buck converter for DDR memory termination

Datasheet - production data



QFN20 3.5 x 4.0 mm

Features

- Integrated MOSFETs for high efficiency
- Current COT architecture
- 1 V to 3.5 V input voltage (V_{IN})
- 5.0 V supply voltage (V_{CC})
- Constant frequency mode
- 1% output voltage accuracy
- Two programmable switching frequencies (0.6 MHz or 1 MHz)
- ADJ output voltage from 0.5 V to 2 V
- Embedded bootstrap diode
- OV/UV/OC and overtemperature protection
- Soft-off with integrated discharge resistor
- External tracking
- Power Good output
- QFN20 3.5 x 4.0 mm compact package

Applications

- Memory termination regulator for DDR3, DDR4 and low power DDR3/DDR4
- Notebook/desktop/server
- Low voltage application for 1 V to 3.5 V input rails

Description

The PM8908 is a high efficiency monolithic step-down switching regulator designed mainly for the DDR termination.

The IC operates from 1 V to 3.5 V input voltage (V_{IN}).

The device uses a COT control loop that provides very good performances in terms of load and line transients. The current sense is internally thermally compensated for optimum precision.

The output voltage is adjusted from 0.5 V to 2 V with ± 1% accuracy overtemperature variations.

The PM8908 also provides external tracking support.

The PM8908 provides positive and negative overcurrent protection as well as over/undervoltage and overtemperature protection. PGOOD output easily provides real-time information on the output voltage.

The PM8908 is available in a QFN20 3.5 x 4.0 mm package.

Table 1. Device summary

Order code	Package	Packaging
PM8908TR	QFN20 (3.5 x 4.0 mm)	Tape and reel

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Contents

1 **Typical application circuit and block diagram 4**

1.1 Application circuit 4

1.2 Block diagram 5

2 **Pin description and connection diagrams 6**

Pin description 6

3 **Thermal data 8**

4 **Electrical specifications 9**

4.1 Absolute maximum ratings 9

4.2 Electrical characteristics 10

5 **Device description 13**

5.1 Power section 13

5.2 Device configuration 14

5.3 Startup and shutdown management 14

Soft-off 16

5.4 Output voltage monitoring and protection 16

5.4.1 Overvoltage protection 16

5.4.2 Undervoltage protection 17

5.4.3 Power Good (PGOOD) 17

5.4.4 Overcurrent protection 17

5.4.5 Overtemperature protection 18

6 **Application information 19**

6.1 Output voltage setting 19

6.2 Droop setting 19

6.3 Non-droop setting 20

6.4 Inductor design 20

6.5 Output capacitors 21

6.6 Input capacitors 21

6.7 Compensation network 22

Prerelease product(s)

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7 Package information 23

7.1 QFN20 package information 24

8 Revision history 27

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1 Typical application circuit and block diagram

1.1 Application circuit

Figure 1. Typical application circuit

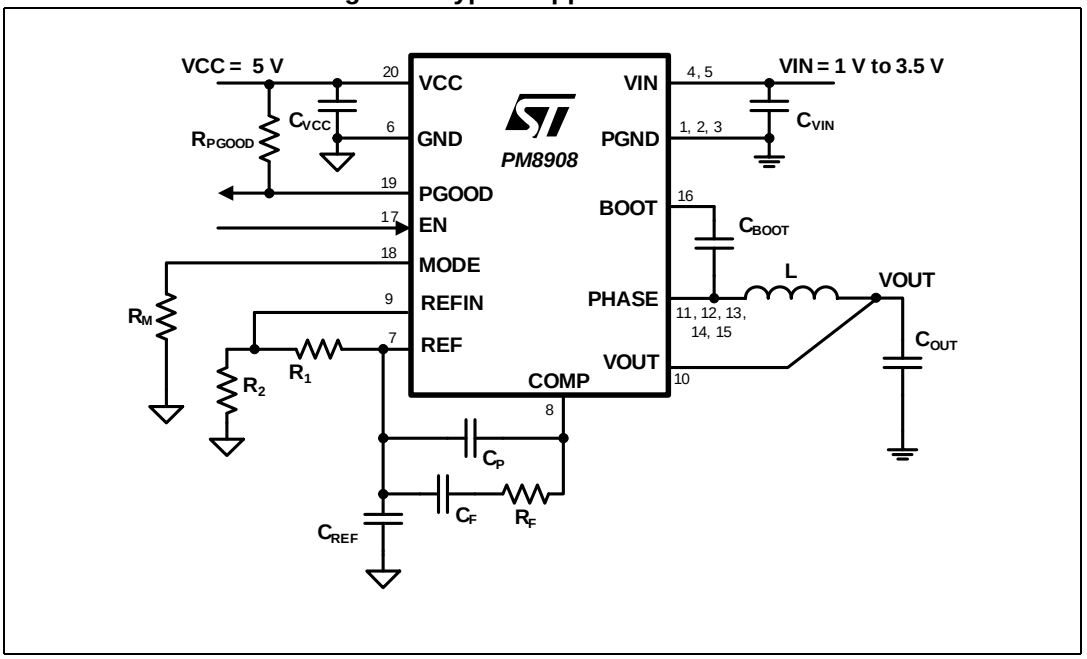
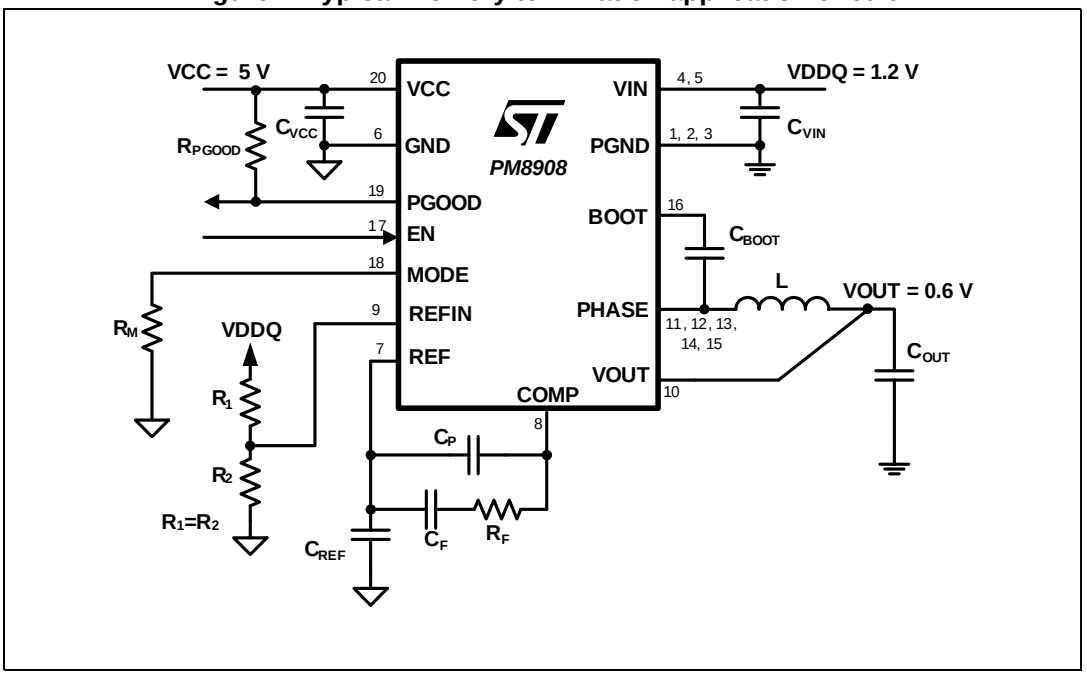


Figure 2. Typical memory termination application circuit

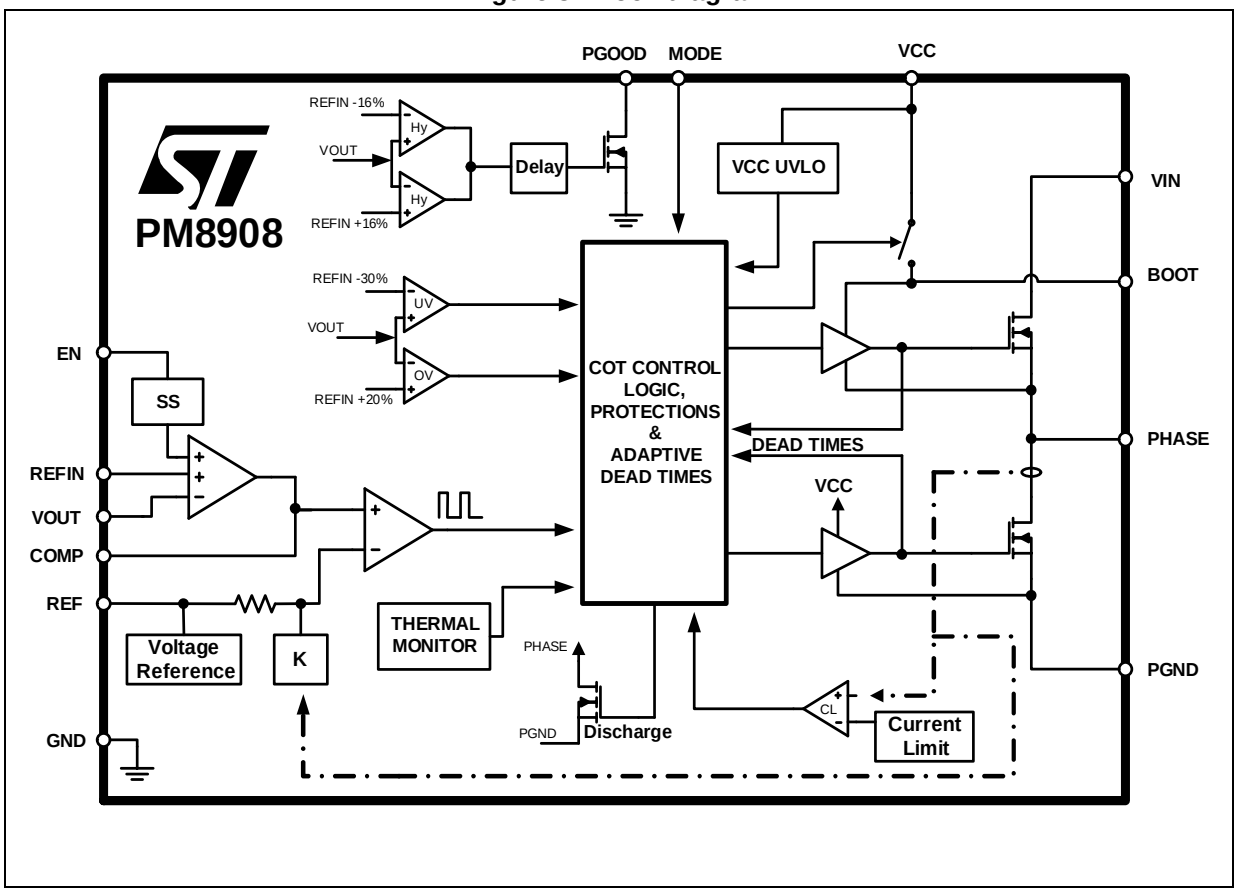


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1.2 Block diagram

Figure 3. Block diagram

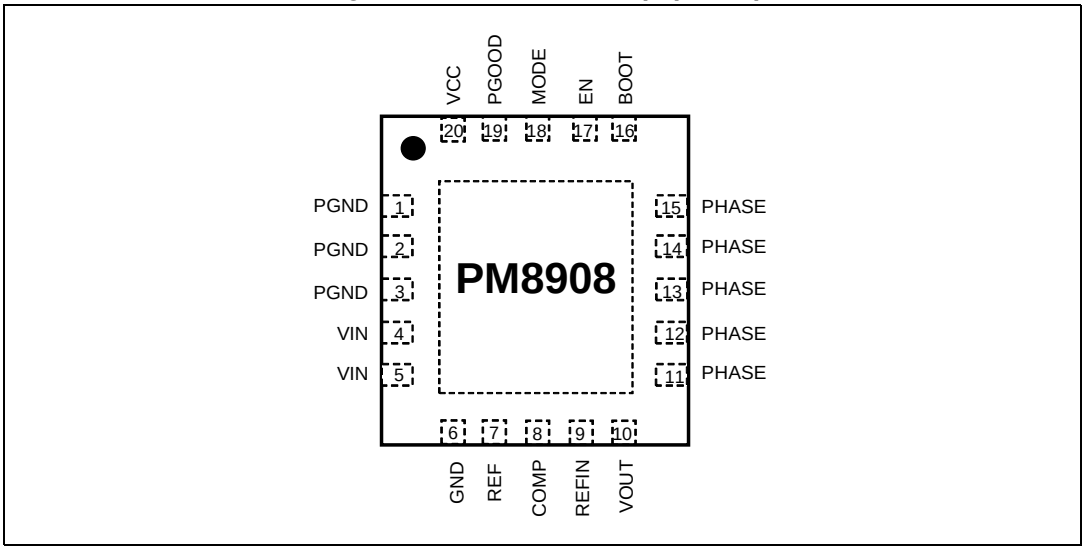


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2 Pin description and connection diagrams

Figure 4. Pin connection (top view)



Pin description

Table 2. Pin description

Pin		Function
No.	Name	
1	PGND	Power ground connection, connected to the embedded low-side MOSFET source. Connect to the PGND PCB plane. See *Figure 1*.
2		
3		
4	VIN	Power input voltage, connected to the embedded high-side MOS drain. Supply range is from 1 V to 3.5 V. Bypass VIN pins to PGND pins close to the IC package with high quality MLCC capacitors. See *Figure 1*.
5		
6	GND	All the internal references are referred to this pin. Connect to the PCB signal ground.
7	REF	Reference output. Connect a 1 µF MLCC capacitor to GND. See *Figure 1*.
8	COMP	Error amplifier output. Connect with R_F - C_F to the REF pin for loop compensation. See *Figure 1*.
9	REFIN	Reference input. Apply a voltage between 0.5 to 2.0 V. Filter with at least 0.01 µF MLCC capacitors to GND.
10	VOUT	Output voltage sense.

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Table 2. Pin description (continued)

Pin		Function
No.	Name	
11	PHASE	Output inductor connection. The pins are connected to the embedded MOSFETs (high-side source and low-side drain). Connect directly to the output inductor. See *Figure 1*.
12		
13		
14		
15		
16	BOOT	Bootstrap pin. It provides power supply for the floating high-side MOS driver. Connect with 0.1 µF to PHASE. See *Figure 1*.
17	EN	Enable.
18	MODE	Switching frequency and the OCL programming pin. See *Table 6 on page 14*. This pin must not be left floating.
19	PGOOD	Power Good pin. Open drain output set free after SS has finished and pulled low when V_{OUT} is out of the PGOOD window or any protection is triggered. Pull up to VCC, if not used it can be left floating.
20	VCC	Device power supply. Operative voltage is 5.0 V. Filter with at least 1 µF MLCC vs. GND.
	Thermal pad	The thermal pad of the device. Connect to the PCB ground plane with multiple VIAS.

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3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient (Device soldered on demonstration board)	40	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Junction temperature range	-40 to 150	°C

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4 Electrical specifications

4.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value(1)	Unit
VCC	To PGND, GND	-0.3 to 7	V
VIN	To PGND, GND	-0.3 to 4	V
BOOT	To PGND, GND	-0.3 to 11	V
	To PGND, GND, t < 10 ns	-0.3 to 12.2(2)	V
	To PHASE	-0.3 to 7	V
PHASE	To PGND, GND	-2 to 4	V
	To PGND, GND, t < 10 ns	-2.2 to 7.5(2)	V
PGOOD	To PGND, GND	-0.3 to 7	V
EN	To PGND, GND	-0.3 to 7	V
VOUT	To PGND, GND	-1.0 to 3.6	V
REFIN, COMP, REF, MODE	To GND	-0.3 to 3.6	V

1. All voltages need to be lower than V_{CC} under any condition.
2. Regardless of application configuration, it is mandatory not to exceed the AMR voltage value on the BOOT and PHASE pins.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal.

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4.2 Electrical characteristics

V_{CC} = 5.0 V ± 5%, T_A = 70°C (unless otherwise specified).

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and undervoltage lockout						
I_{IN}	VIN shutdown current	Shutdown, EN = 0 V		0.3	5	µA
I_{CC}	V_{CC} supply current	EN = H, V_{BOOT} = 4.5 V, V_{CC} = 4.5 V, V_{IN} = 3.5 V, V_M = GND		2	3.6	mA
I_{CCSD}	V_{CC} shutdown current	Shutdown, EN = 0 V		4	10	µA
I_{BSS}	Boot input current	V_{BOOT} = 9 V, V_{PHASE} = 3.5 V, V_{CC} = 5.5 V			150	µA
V_{CC}	V_{CC} supply voltage		4.5	5.0	5.5	V
V_{CC} UVLO	V_{CC} turn-on	V_{CC} rising	4.2	4.37	4.5	V
	Hysteresis			440		mV
REF UVLO	V_{REF} turn-on	REF rising		1.8		V
	Hysteresis			100		mV
Oscillator, off-time and on-time						
f_{SW}	Oscillator accuracy	R_M = 100 kΩ		1		MHz
		R_M = 47 kΩ		0.6		
$t_{OFF-min}$	Minimum off-time	V_{IN} = 1.5 V, V_{OUT} = 0.9 V, V_{REFIN} = 1 V, f_{SW} = 1 MHz / 0.6 MHz		170		ns
Reference and GM amplifier						
ΔV_{OUT}	Output voltage accuracy	V_{REFIN} = 1 V, no droop	-1		+1	%
V_{REF}	Voltage reference	I_{REF} = 0	1.95	2.0	2.05	V
G_M	Transconductance(1)			1.00		mS
I_{CSK}	COMP pin maximum sinking current	V_{COMP} = 2 V, V_{REFIN} - V_{OUT} = -80 mV		80		µA
I_{CSR}	COMP pin maximum sourcing current	V_{COMP} = 2 V, V_{REFIN} - V_{OUT} = 80 mV		-80		µA
V_{CM}	Common mode input voltage range(1)		0		2	V
V_{DM}	Differential mode input voltage range(1)		0		80	mV
V_{OSet}	Input offset			0		mV
F_{-3dB}	-3 dB frequency(1)		4.5	6.0	7.5	MHz
A_{CS}	Current sense gain	Gain from the current of the LS to PWM comp when PWM = OFF	47.3		59.3	mV/A

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Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Soft-end						
R_{DS}	Phase discharge resistance			51		Ω
Overcurrent protection						
I_{OCL}	Positive overcurrent threshold	LS sourcing, R_M = 47 kΩ	4	7.6	11	A
I_{OCLN}	Negative overcurrent threshold	LS sourcing, R_M = 47 kΩ	-11	- 7.6	- 4	A
Bootstrap switch						
R_{BSS}	Boot switch on-resistance	I_{BOOT} = 10 mA, T_A = 25 °C			12.6	Ω
Over and undervoltage protection						
OVP	OVP threshold	V_{OUT} rising	117	120	123	% V_{REFIN}
t_{OVPd}	OVP delay	Time from the V_{OUT} pinout of + 20% of REFIN to OVP fault		10		µs
UVP	UVP threshold	V_{OUT} falling	65	68	71	% V_{REFIN}
t_{UVPd}	UVP delay	Time from the V_{OUT} pinout of -30% of REFIN to UVP fault		256		µs
	Undervoltage fault enable delay	Time from EN = H to undervoltage ready		2.4		ms
		External tracking Time from EN = H to undervoltage ready		9		ms
Overtemperature protection						
OTP	Thermal shutdown threshold(1)			145		°C
	Thermal shutdown hysteresis(1)			10		°C
PGOOD						
PGOOD	Upper threshold	V_{OUT} rising		116		% V_{REFIN}
		Hysteresis		8		
	Lower threshold	V_{OUT} falling		84		
		Hysteresis		8		
$V_{PGOOD,L}$	PGOOD voltage low impedance	I_{PGOOD_SINK} = 4 mA, V_{CC} = 4.5 V			0.338	V
$I_{PGOOD,H}$	PGOOD leakage high impedance	V_{PGOOD} = 5.5 V			1	µA
t_{PGd}	PGOOD startup delay time	External tracking Time from EN = H to PGOOD high		10		ms
t_{PGHd}	PGOOD high delay time	Rising edge	0.8	1	1.2	ms
t_{PGLd}	PGOOD low delay time	Falling edge(2)		10		µs

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Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ENABLE						
EN	Input logic high	EN rising	2			V
	Input logic low	EN falling			0.5	V
I_{EN}	EN input current	V_{EN} = 5 V			3	µA
MODE						
I_M	Mode current	V_{MODE} from GND to 2.4 V		15		µA
SOFT-START						
t_{SS}	Soft-start time	From EN = H to V_{OUT}		2.4		ms
td	Delay soft-start time	From EN = H to V_{OUT} ramp starts		750		µs

1. Guaranteed by design, not subject to test.
2. Delay time not valid if the UVLO or EN shutdown events are occurring.

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5 Device description

The PM8908 is a high efficiency synchronous step-down monolithic switching regulator capable to deliver or sink the current.

The power input voltage (VIN) can range from 1 V to 3.5 V, the signal input voltage (VCC) can range from 4.5 V to 5.5 V.

The output voltage is regulated to the REFIN voltage which comes from an external reference voltage. The output voltage accuracy is better than ± 1% over the line, load and temperature.

The PM8908 embeds low $R_{DS(on)}$ N-channel MOSFETs for both HS (high-side) and LS (low-side).

The high-switching frequency selectable in two values - 600 kHz or 1 MHz and the small package allows very compact VR solutions.

In the COT the t_{ON} is function of V_{IN}, V_{OUT} and switching frequency (f_{SW}), as shown in *Equation 1*:

Equation 1

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \cdot f_{SW}}$$

The PM8908 features a full set of protections and output voltage monitoring:

- Precise and accurate overcurrent limit (internally compensated against temperature variations)
- Over and undervoltage protection
- Overtemperature protection
- Undervoltage lockout on analog supply (VCC)
- Power Good open drain output easily provides real-time information about the output voltage.

The dedicated ENABLE pin (EN) offers easy control on the power sequencing. Forcing the EN low, the device enters the shutdown state and absorbs a total quiescent current from VCC and VIN less than 15 µA.

5.1 Power section

The PM8908 integrates two low $R_{DS(on)}$ N-channel MOSFETs as low-side and high-side switches, optimized for fast switching transition and high efficiency over the entire load range.

The HS MOSFET drain is connected to the VIN pins (power input), the LS MOSFET source is connected to the PGND pins (power ground), and the HS MOSFET source and LS MOSFET drain are connected together and to the PHASE pins (see *Figure 1 on page 4*). The driving section is supplied from the VCC pins that assure the proper driving voltage over all the VIN range.

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To properly supply the power section is advised following:

- Bypass VIN pins to PGND pins as close as possible to the IC package with high quality MLCC capacitors.
- Connect the bootstrap capacitor (typically a 100 nF ceramic capacitor rated to stand VIN voltage) from the BOOT pin to the PHASE pin to supply the HS driver.

Caution: Do not connect an external bootstrap diode. The IC already integrates an active bootstrap switch to charge the bootstrap capacitor, saving the cost of this external component.

The PM8908 embodies the anti shoot-through and adaptive deadtime control to minimize low-side body diode conduction time and consequently to reduce power losses:

- When the gate driving voltage of the HS drops (to check high-side MOSFET turn-off), the LS MOSFET is suddenly switched on
- When the gate driving voltage of the LS drops (to check low-side MOSFET turn-off), the HS MOSFET is suddenly switched on.

5.2 Device configuration

The PM8908 has a programming pin - MODE (pin 18) - which allows choosing the regulator switching frequency and the OCL threshold. This programming feature is performed by selecting the proper resistor, to be mounted between the pin 18 to ground, as summarized in *Table 6*.

Table 6. Switching frequency and OCL (see *Figure 1 on page 4*)

R_M	f_{SW} [kHz]	OCL (A)
47 kΩ	600	7.6
68 kΩ	600	5.4
100 kΩ	1000	5.4

Note: The MODE pin must not be left floating.

5.3 Startup and shutdown management

The IC monitors the supply voltage on the VCC pin. Once VCC voltage is above the UVLO (undervoltage lockout) threshold and the EN pin is above the turn-on threshold:

- If the IC is configured for tracking application (see *Figure 2 on page 4*), the output voltage is regulated to the REFIN voltage. In order to discriminate between the non-tracking and the tracking, there is a delay time of 750 µs required between the EN or the VCC UVLO threshold and REFIN voltage. REFIN voltage must be applied within 9 ms (typ.) from the EN high (see *Figure 5*).
- If the IC is configured for non-tracking application, the output voltage is regulated to the REFIN voltage, and the device provides a precise 2.4 ms soft-start time (see *Figure 6*).

The power input (VIN) does not have a undervoltage protection function.

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Figure 5. PM8908 turn-on (tracking startup)

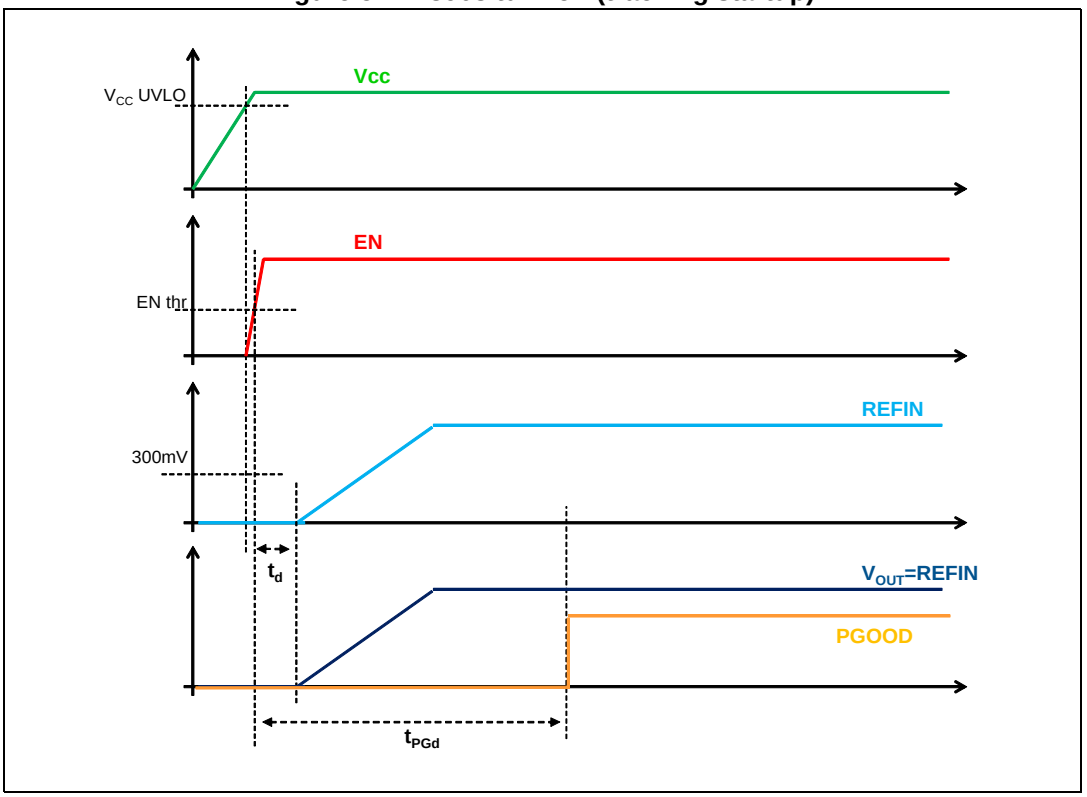
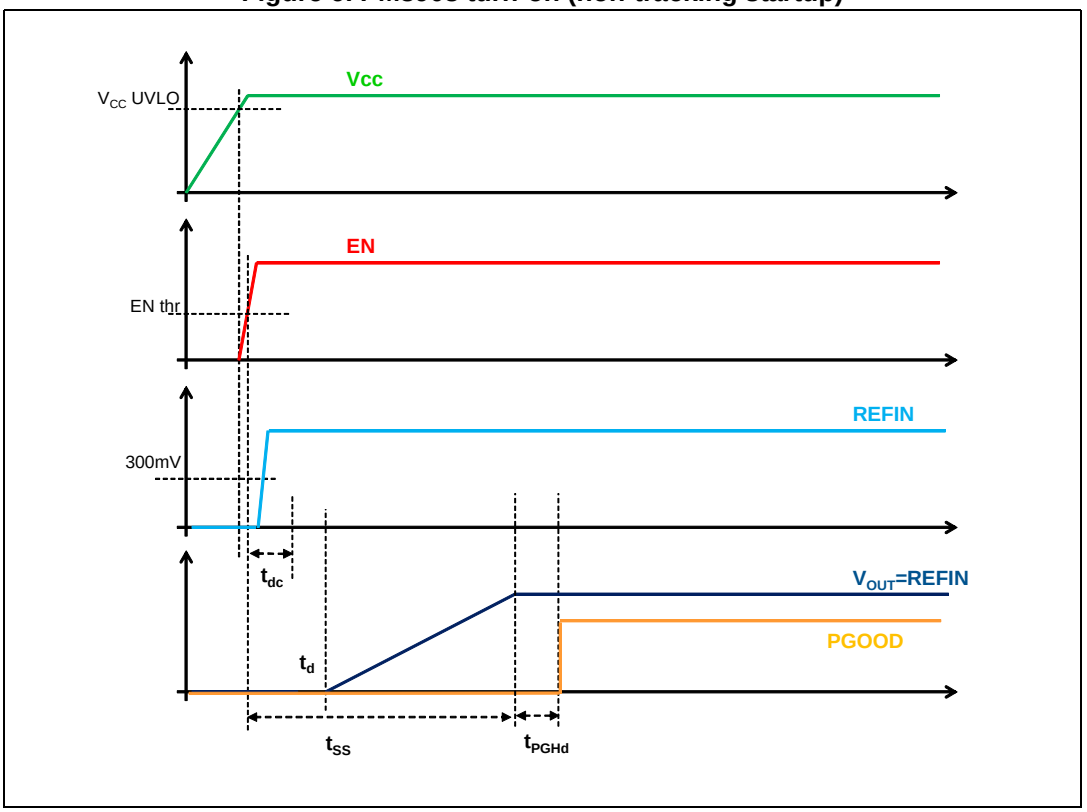


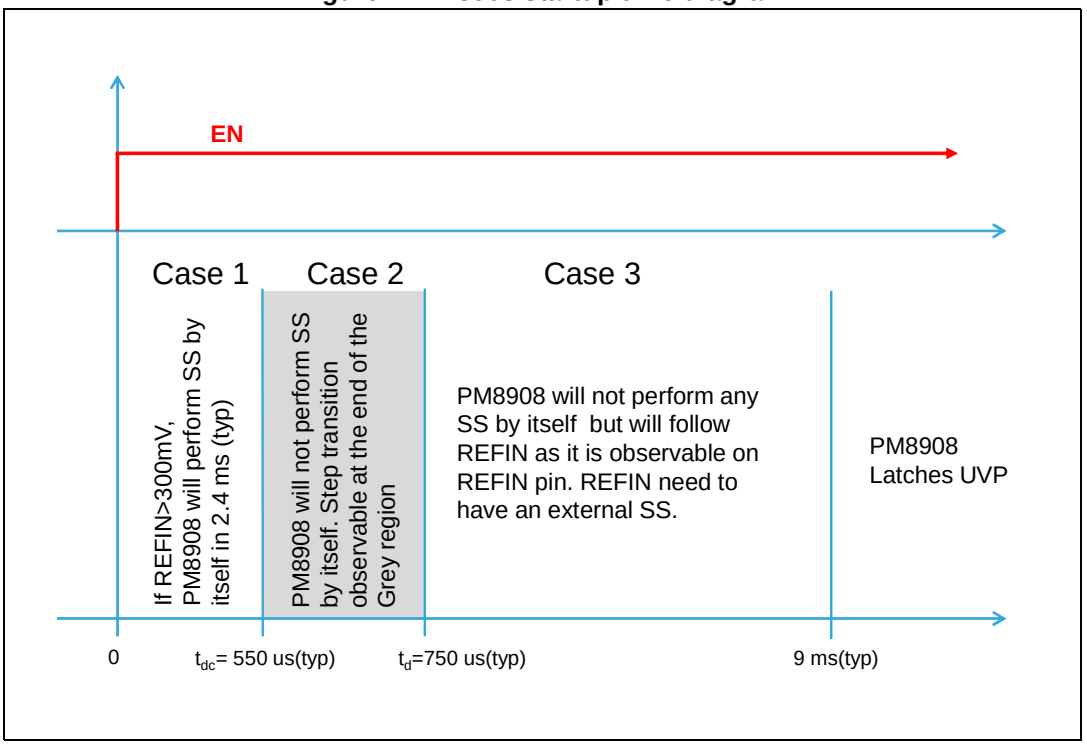
Figure 6. PM8908 turn-on (non-tracking startup)



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Figure 7. PM8908 startup time diagram



Soft-off

The PM8908 implements the soft-off sequence turning off both the HS and LS MOSFETs and connecting the integrated discharge resistor (47 Ω) between the PHASE and PGND pin.

The PM8908 begins the soft-off sequence, and remains in a latched state, if one of the following conditions occurs:

- VCC voltage falls below UVLO threshold
- OVP (overvoltage protection)
- UVP (undervoltage protection)
- EN pin is pulled low.

The cycling VCC and EN the IC recover from the latched state with a new soft-start sequence.

5.4 Output voltage monitoring and protection

The PM8908 monitors the output voltage status through the V_{OUT} pin and compares the voltage on this pin with the REFIN voltage in order to provide over and undervoltage protection as well as the PGOOD signal.

5.4.1 Overvoltage protection

Overvoltage protection is active as soon as the device is enabled, the VCC is above the respective undervoltage lockout level and REFIN is higher than 300 mV.

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The protection is triggered when the voltage sensed on the V_{OUT} pin rises over the OVP threshold and the device acts as follows:

- De-asserts the PGOOD signal
- The HS MOSFET is suddenly forced OFF
- The LS MOSFET is turned on (to discharge the output and protect the load). When V_{OUT} drops below the UVP threshold the LS MOSFET is turned off and the discharge resistor is on. If V_{OUT} recrosses the UVP threshold, the LS is turned on again and the discharge resistor is off.

In the overvoltage protection state the negative overcurrent limit (OCLN) is masked.

This protection is latched, cycled EN or VCC to recover.

5.4.2 Undervoltage protection

If VOUT falls below the UVP threshold for at least 256 µs the IC stops switching and starts a soft-off sequence.

The device acts as follows:

- De-asserts the PGOOD signal
- The HS MOSFET and LS MOSFET are forced OFF
- The discharge resistor is on.

This protection is latched, cycled EN or VCC to recover.

The UVP protection is enabled after the soft-start end.

5.4.3 Power Good (PGOOD)

The PGOOD is an open drain output. During the startup, the PGOOD goes high after 1 ms from the threshold detected.

The PGOOD is forced low, to communicate that the output voltage is no longer in regulation, if one of the following conditions is verified:

- The voltage of the V_{OUT} pin exits from the PGOOD window
- The device is disabled, EN is forced low
- VCC voltage is below the UVLO threshold
- Any protection is triggered (OVP, UVP, OTP).

5.4.4 Overcurrent protection

Overcurrent protection is active as soon as the device is enabled and VCC voltage is above the UVLO level.

The overcurrent function protects the converter from a shorted output or overload by sensing the output current information across the low-side integrated MOSFET.

- Positive OCL

If the monitored current information is bigger than the overcurrent thresholds, an overcurrent event is detected. The IC delays the next t_{ON} until the current drops below the positive OCL limit.

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The maximum available load current, with the valley current limit technique, is equal to *Equation 2*:

Equation 2

$$I_{LOADmax} = I_{OCL} + \frac{1}{2} \cdot \Delta I$$

It is the sum of the valley current limit plus the half of the inductor current ripple.

During the overcurrent event the Vout drops until the UVP threshold, de-asserts the PGOOD pin and then enters into the latch state.

- Negative OCL

The negative OCL circuit operates when the converter is sinking the current from the output load. The IC trigs the next t_{ON} until the current drops below the negative OCL limit.

During the overcurrent event the Vout goes up until the OVP threshold, de-asserts the PGOOD pin and then enters into the latch state.

5.4.5 Overtemperature protection

It is recommended that the device never exceeds the maximum allowable junction temperature. This temperature increase is mainly caused by the total power dissipated from the integrated power MOSFETs.

To avoid any damage to the device when reaching high temperature, the PM8908 implements a thermal shutdown feature: when the junction temperature reaches 145 °C the device turns off both MOSFETs. When the junction temperature drops to 135 °C, the device restarts with a new soft-start sequence.

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6 Application information

6.1 Output voltage setting

The PM8908 integrates a 2 V internal reference (V_{REF}), with the total accuracy of ± 1%.

The output voltage, in non-tracking configuration, can be easily programmed connecting the R_1 and R_2 resistors as follows (see also *Figure 8*).

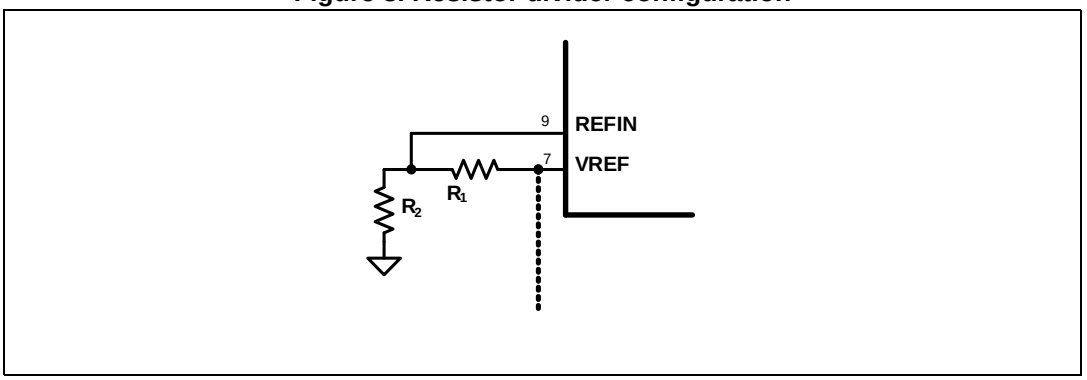
- Connect the REFIN to the REF pin through the R_1 resistor
- Connect the REFIN pin to the GND through the R_2 resistor

Therefore, the output voltage setting is easily achieved using *Equation 3* to select the value of the R_{OS} resistor:

Equation 3

$$V_{OUT} = \frac{V_{REF}}{1 + (R_1 / R_2)}$$

Figure 8. Resistor divider configuration



6.2 Droop setting

In order to reduce the necessary output capacitance amount, the PM8908 can perform the load dependent behavior if the compensation network capacitor, CC, is avoided. The sensed current is used for reference voltage, in the PWM comparator inverting input. So doing, the programmed output voltage is:

Equation 4

$$V_{OUT} = V_{REFIN} - V_{DROOP}$$

where: $V_{DROOP} = \frac{A_{CS} \cdot I_{LOAD}}{R_{DROOP} \cdot G_M}$

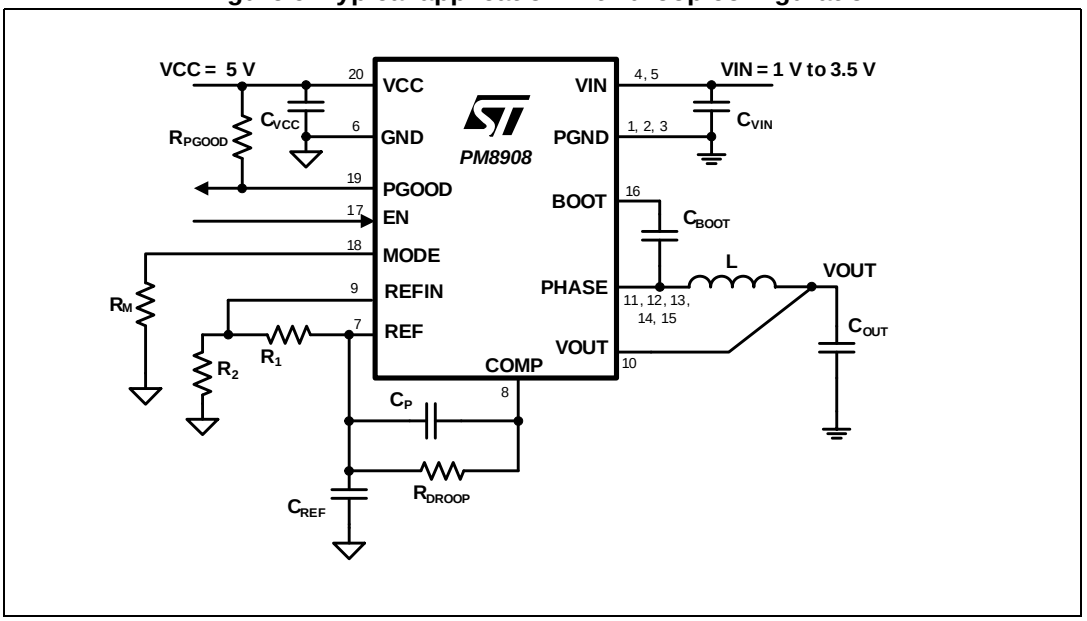
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with:

- R_{DROOP} is the resistor between the COMP pin and the REF pin (see also *Figure 9*)
- I_{LOAD} is the output current
- G_M is the transconductance of the amplifier (1 mS)
- A_{CS} is the current sense gain (53 mV/A)

Figure 9. Typical application with droop configuration



6.3 Non-droop setting

The advantage of a non-droop configuration is that the load regulation is flat. It can be implemented by connecting a resistor (R_C) and a capacitor (C_C) between the COMP pin and the REF pin (see also *Figure 1 on page 4*).

6.4 Inductor design

The inductance value is defined by a compromise between the dynamic response time, the efficiency, the cost, and the size. The inductor must be calculated to maintain the ripple current (ΔI_L) between 20% and 30% of the maximum output current (typ.). The inductance value can be calculated with the following relationship:

Equation 5

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

where f_{SW} is the switching frequency, V_{IN} is the input voltage, and V_{OUT} is the output voltage.

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6.5 Output capacitors

The output capacitors are basic components to define the ripple voltage across the output and for the fast transient response of the power supply. They depend on the output voltage ripple requirements, as well as any output voltage deviation requirement during a load transient.

During steady-state conditions, the output voltage ripple is influenced by both the ESR and the capacitive value of the output capacitors as follows:

Equation 6

$$\Delta V_{OUT_ESR} = \Delta I_L \cdot ESR$$

Equation 7

$$\Delta V_{OUT_C} = \Delta I_L \cdot \frac{1}{8 \cdot C_{OUT} \cdot F_{SW}}$$

where ΔI_L is the inductor current ripple. In particular, the expression that defines ΔV_{OUT_C} takes into consideration the output capacitor charge and discharge as a consequence of the inductor current ripple.

6.6 Input capacitors

The input capacitor bank is designed considering, mainly, the input RMS current that depends on the output deliverable current (I_{OUT}) and the duty cycle (D) for the regulation as follows:

Equation 8

$$I_{rms} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

The equation reaches its maximum value, $I_{OUT}/2$, with D = 0.5. The losses depend on the input capacitor ESR and, in the worst case, are:

Equation 9

$$P = ESR \cdot (I_{OUT}/2)^2$$

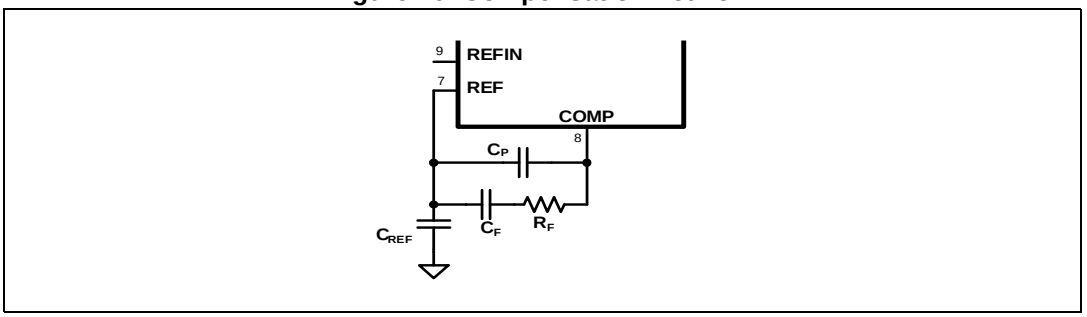
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6.7 Compensation network

The PM8908 device implements a constant on-time control loop. The compensation network is shown in *Figure 10*.

Figure 10. Compensation network



The following procedure shall be followed in order to calculate the best network external components value.

- Select R_F value in order to obtain the desired closed loop regulator bandwidth according to *Equation 10*:

Equation 10

$$R_F = 2\pi \cdot f_T \cdot C_{OUT} \cdot \frac{R_{CS}}{g_M}\left(1 + 2\pi \cdot \frac{f_T}{5} \cdot \frac{ESR \cdot C_{OUT}}{1 - 2\pi \cdot \frac{f_T}{5} \cdot ESR \cdot C_{OUT}}\right)$$

where:

  - f_T is the crossover frequency, it should be less than about 1/10 of the switching frequency
  - R_{CS} = 53 mΩ
- Select C_F according to *Equation 11*:

Equation 11

$$C_F \geq \frac{1}{2\pi \cdot \frac{f_T}{5} \cdot R_F}$$

- Select C_P according to *Equation 12*:

Equation 12

$$C_P = \frac{ESR \cdot C_{OUT}}{R_C \cdot \left(1 - 2\pi \cdot \frac{f_T}{5} \cdot ESR \cdot C_{OUT}\right)}$$

- Check the phase margin obtained and repeat the whole procedure if necessary.

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7 Package information

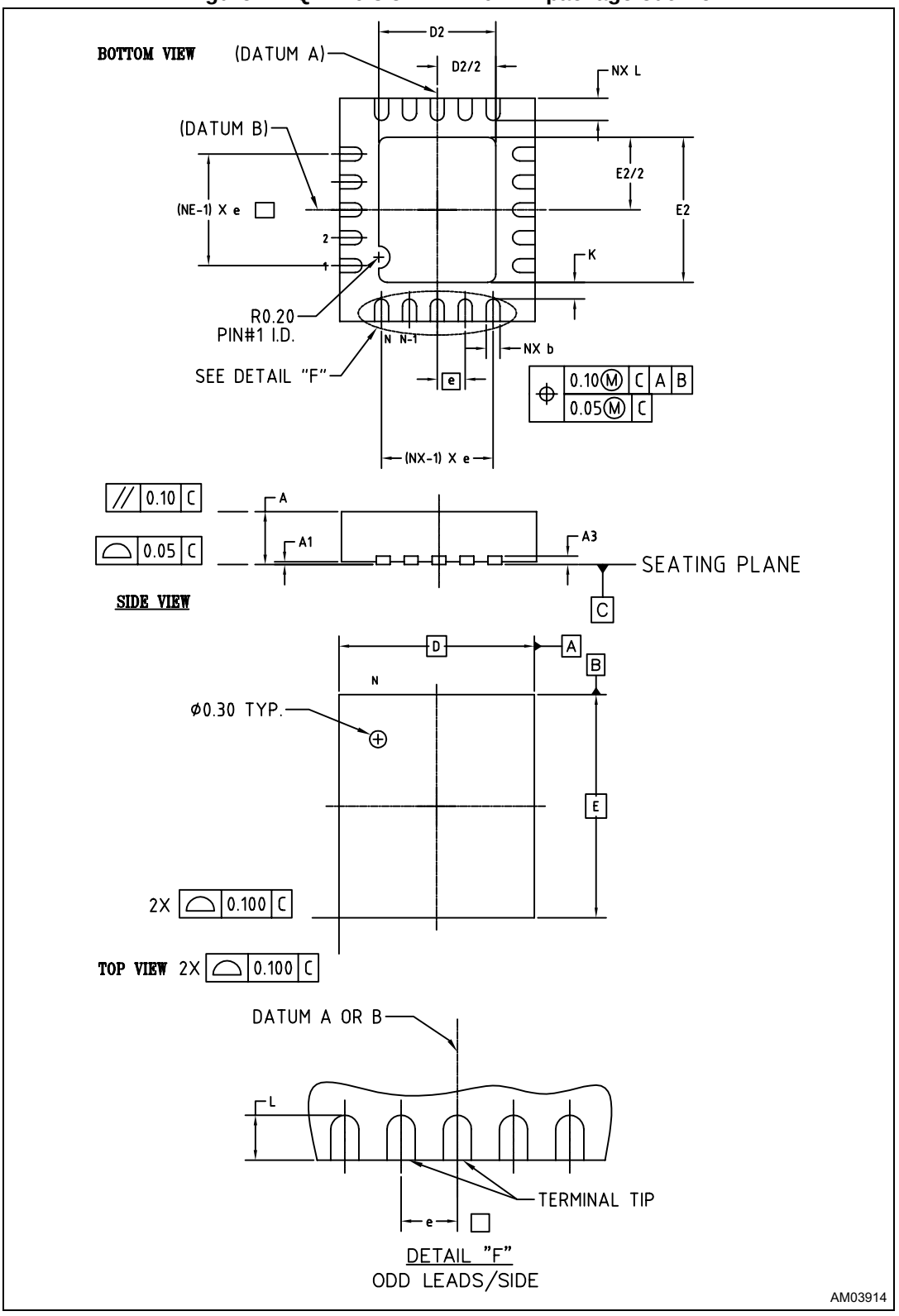
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*.
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7.1 QFN20 package information

Figure 11. QFN20 3.5 x 4 x 1.0 mm package outline



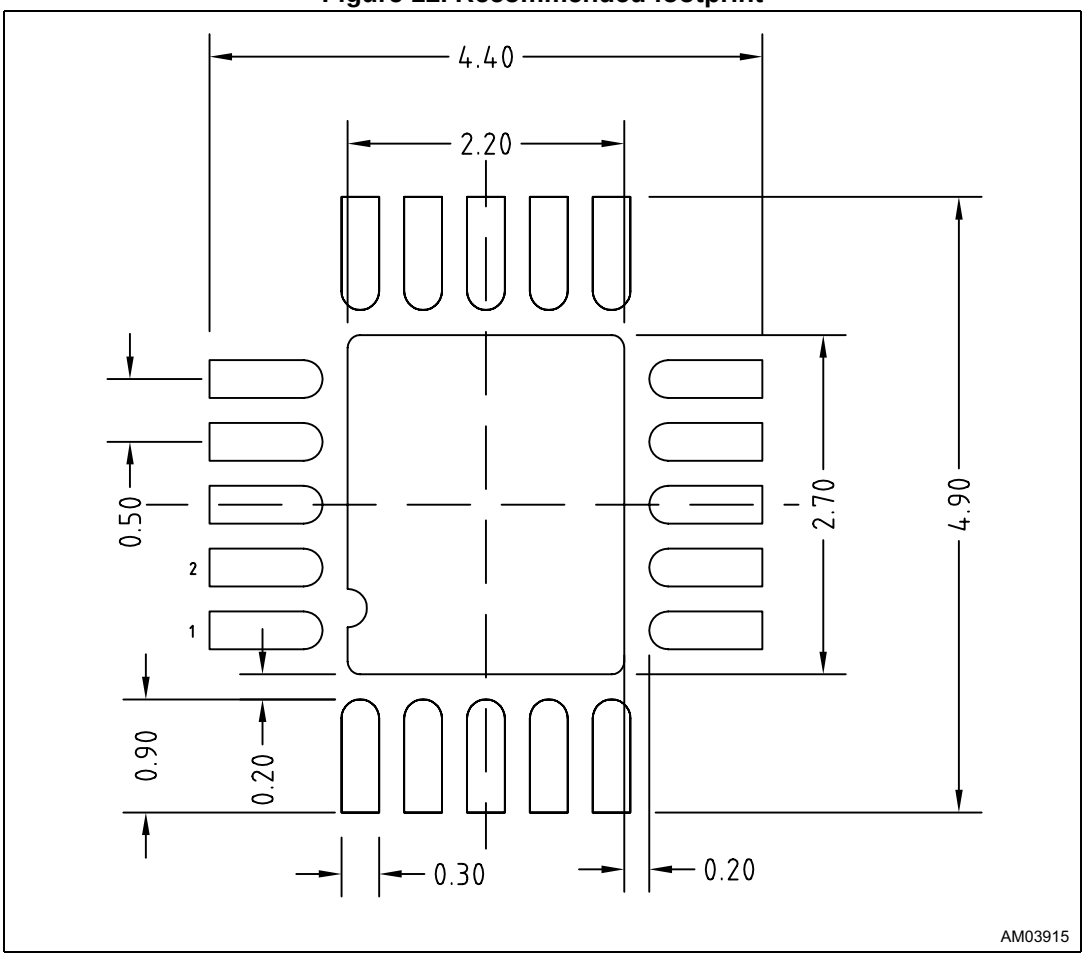
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Table 7. QFN20 3.5 x 4 x 1.0 mm package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1	0.00	0.02	0.05
A3		0.152	
b	0.18	0.25	0.30
D	3.4	3.5	3.6
D2	2.00	2.10	2.20
E	3.9	4.0	4.1
E2	2.50	2.60	2.70
e		0.50	
L	0.35	0.40	0.45
K	0.20		

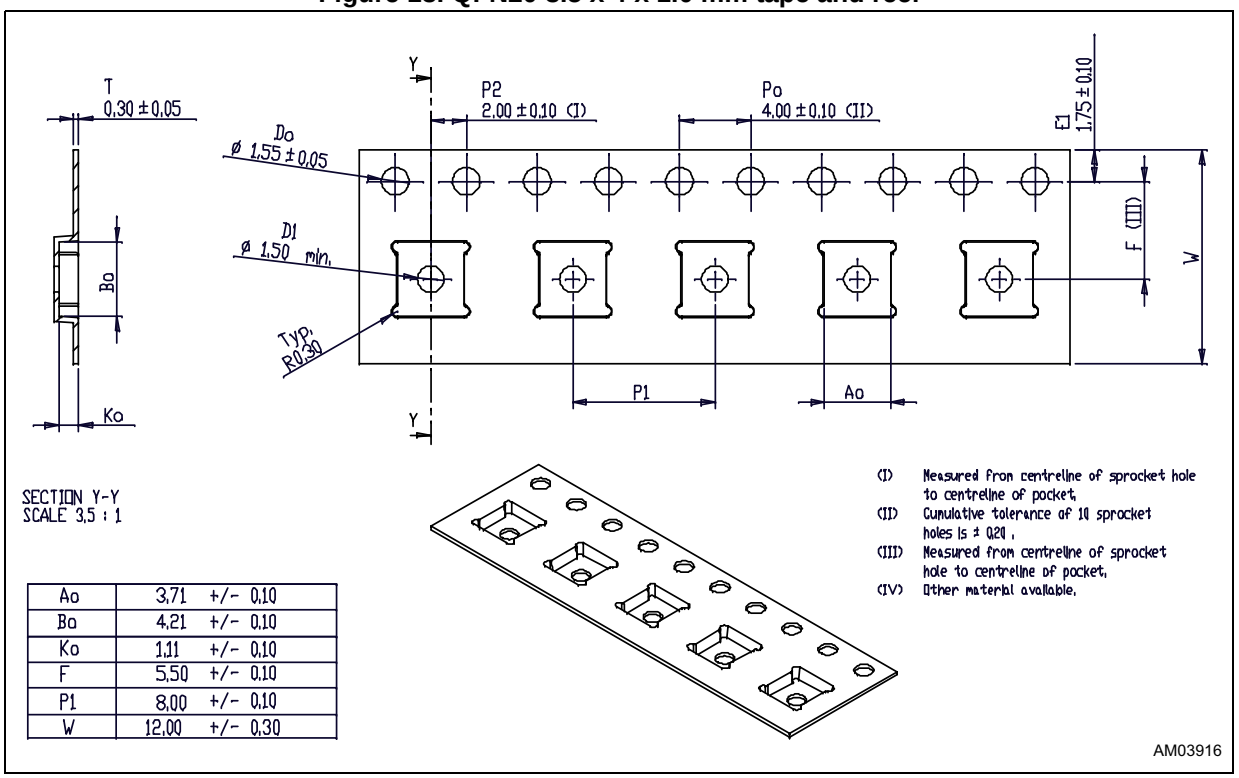
Figure 12. Recommended footprint



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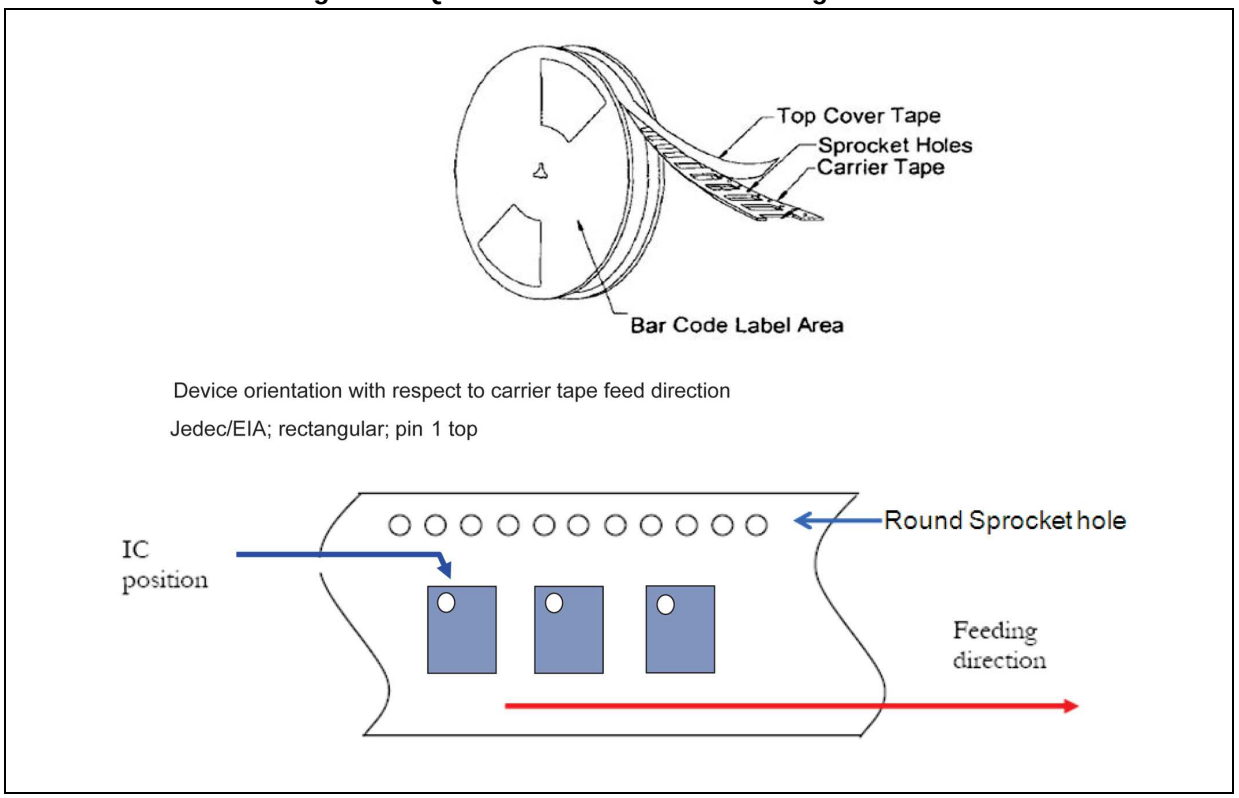
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Figure 13. QFN20 3.5 x 4 x 1.0 mm tape and reel



Ao	3,71	+/- 0,10
Bo	4,21	+/- 0,10
Ko	1,11	+/- 0,10
F	5,50	+/- 0,10
P1	8,00	+/- 0,10
W	12,00	+/- 0,30

Figure 14. QFN20 3.5 x 4 x 1.0 mm winding direction



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8 Revision history

Table 8. Document revision history

Date	Revision	Changes
30-Mar-2015	1	Initial release.
22-Oct-2015	2	– Added footnote *2* to *Table 4*. – Added minimum and maximum dimension values for symbols D and E in *Table 7*.
09-Nov-2015	3	First public release.
25-Jul-2017	4	Updated: A_{CS}, R_{DS}, R_{BSS} and $V_{PGOOD,L}$ values in *Table 5*.

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