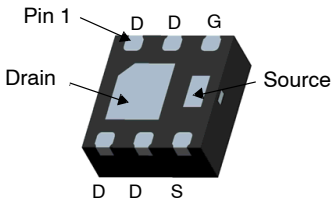
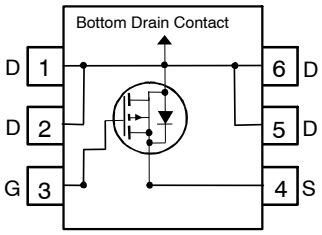
MOSFET – Single P-Channel, POWERTRENCH®, 1.8 V Specified

FDMA291P



WDFN6 (MicroFET 2 x 2)
CASE 511CZ



General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on−state resistance. The MicroFET™ 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- –6.6 A, –20 V
  - $R_{DS(ON)}$ = 42 mΩ @ V_{GS} = –4.5 V
  - $R_{DS(ON)}$ = 58 mΩ @ V_{GS} = –2.5 V
  - $R_{DS(ON)}$ = 98 mΩ @ V_{GS} = –1.8 V
- Low Profile – 0.8 mm Maximum – in the New Package MicroFET 2x2 mm
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb−Free, Halide Free and RoHS Compliant RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

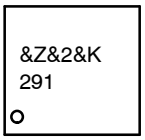
Symbol	Parameter	Value	Unit
V_{DS}	Drain−Source Voltage	–20	V
V_{GS}	Gate−Source Voltage	±8	V
I_D	Drain Current – Continuous (Note 1a) – Pulsed	 –6.6 24	A
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	 2.4 0.9	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	13	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1b)	145	°C/W

MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = 2 Digit Date Code (YW)
&K = 2 Digit Lot Traceability Code
291 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDMA291P	WDFN6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA	–20	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C	–	–12	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V	–	–	–1	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±8 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–0.4	–0.7	–1.0	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate Threshold Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C	–	3	–	mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –4.5 V, I_D = –6.6 A V_{GS} = –2.5 V, I_D = –5.1 A V_{GS} = –1.8 V, I_D = –3.9 A V_{GS} = –4.5 V, I_D = –6.6 A, T_J = 125°C	– – – 	36 51 79 49	42 58 98 64	mΩ
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –6.6 A	–	16	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = –10 V, V_{GS} = 0 V, f = 1.0 MHz	–	1000	–	pF
C_{oss}	Output Capacitance		–	190	–	pF
C_{rss}	Reverse Transfer Capacitance		–	100	–	pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –10 V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω	–	13	23	ns
t_r	Turn–On Rise Time		–	9	18	ns
$t_{d(off)}$	Turn–Off Delay Time		–	42	68	ns
t_f	Turn–Off Fall Time		–	25	40	ns
Q_g	Total Gate Charge	V_{DS} = –10 V, I_D = –6.6 A, V_{GS} = –4.5 V	–	10	14	nC
Q_{gs}	Gate–Source Charge		–	2	–	nC
Q_{gd}	Gate–Drain Charge		–	3	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain–Source Diode Forward Current		–	–	–2	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –2 A (Note 2)	–	–0.8	–1.2	V
t_{rr}	Reverse Recovery Time	I_F = –6.6 A d_{iF}/d_t = 100 A/μs	–	20	–	ns
Q_{rr}	Reverse Recovery Charge		–	8	–	nC

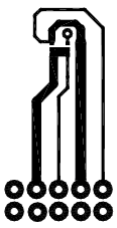
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR–4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 52 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 145 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

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TYPICAL CHARACTERISTICS

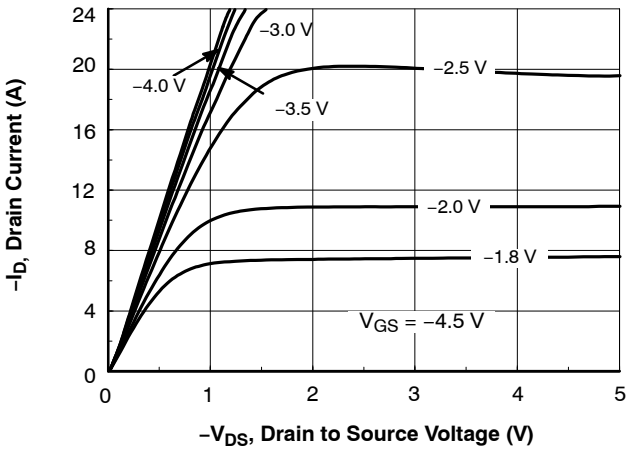


Figure 1. On−Region Characteristics

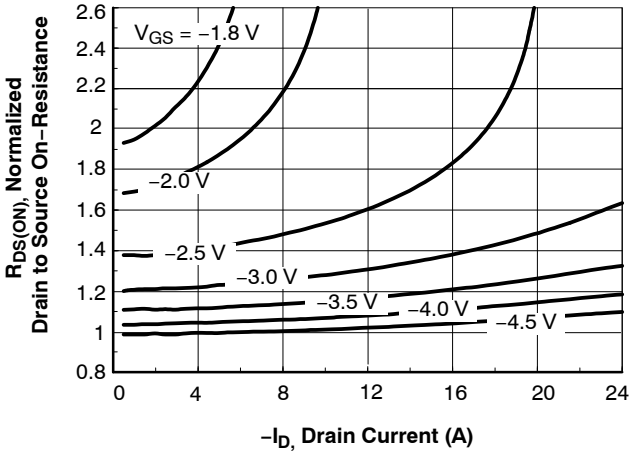


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

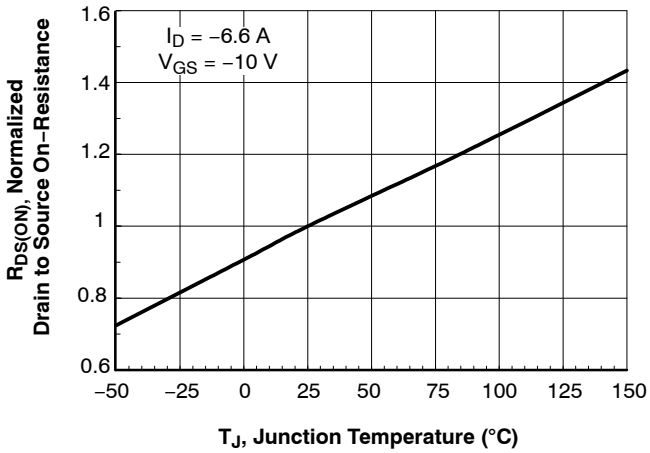


Figure 3. On−Resistance Variation with Temperature.

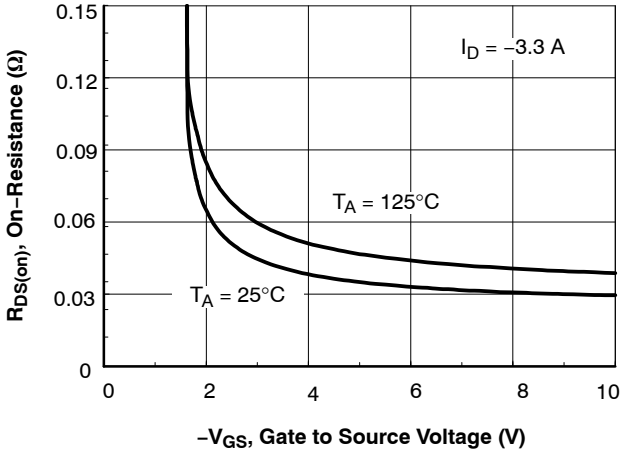


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

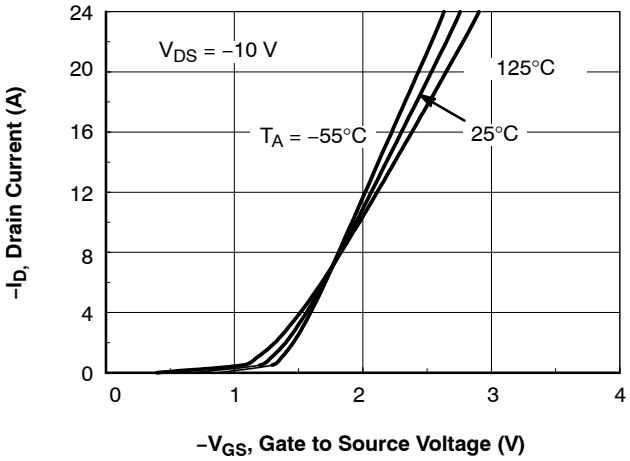


Figure 5. Transfer Characteristics

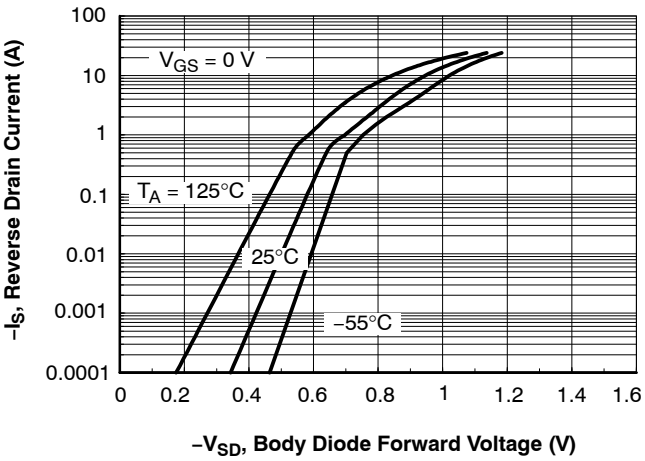


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

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TYPICAL CHARACTERISTICS (Continue)

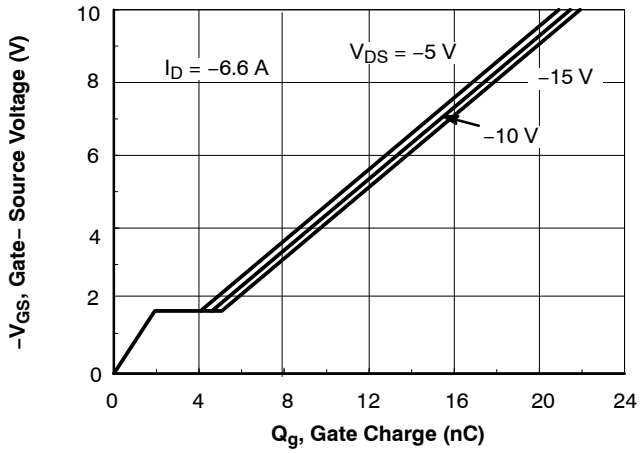


Figure 7. Gate Charge Characteristics

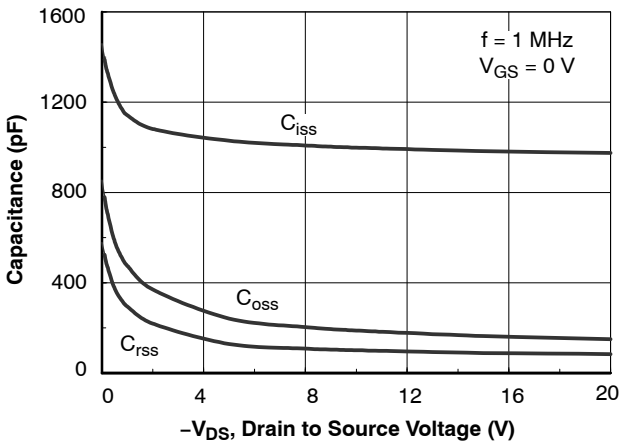


Figure 8. Capacitance Characteristics

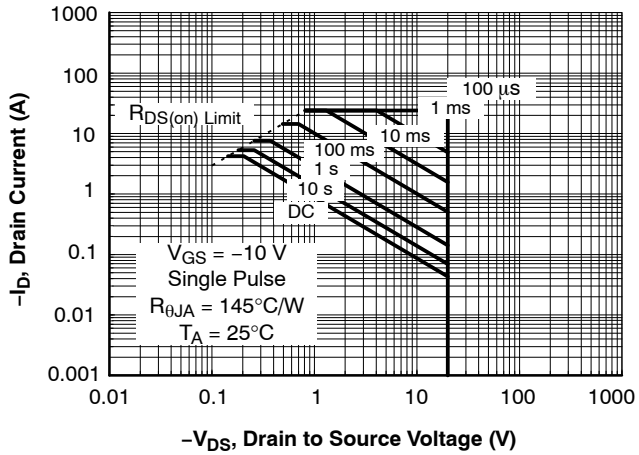


Figure 9. Maximum Safe Operating Area

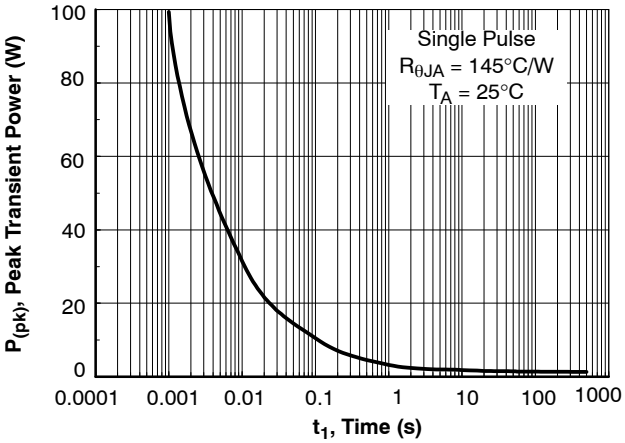


Figure 10. Single Pulse Maximum Power Dissipation

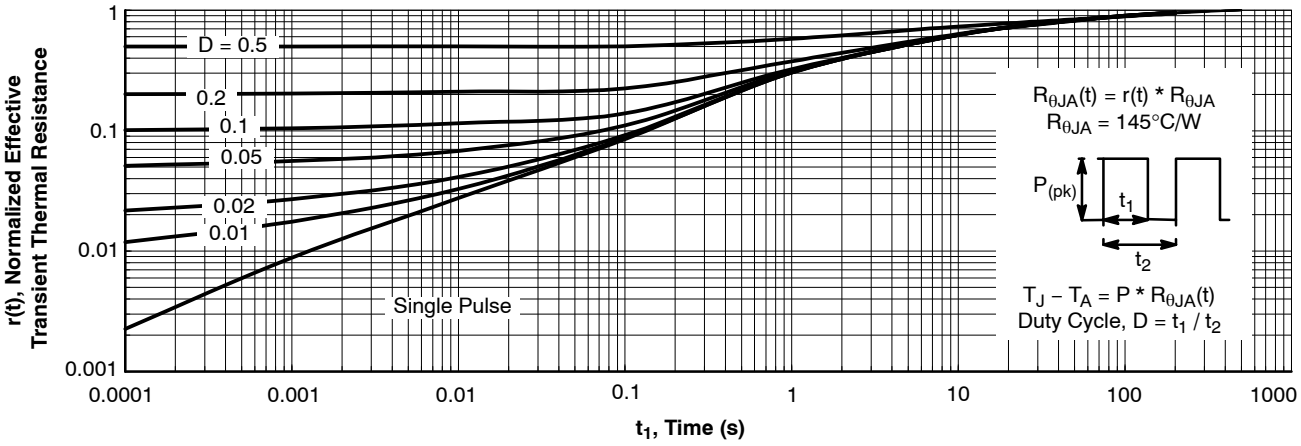


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note1b.
Transient thermal response will change depending on the circuit board design.

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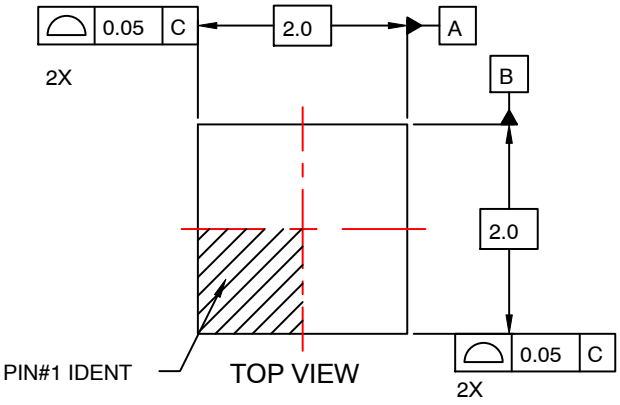
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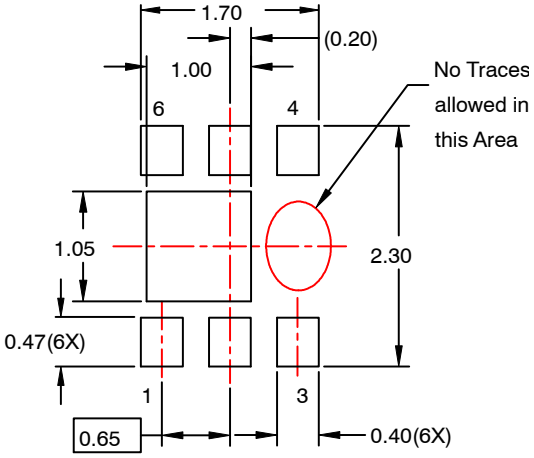
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

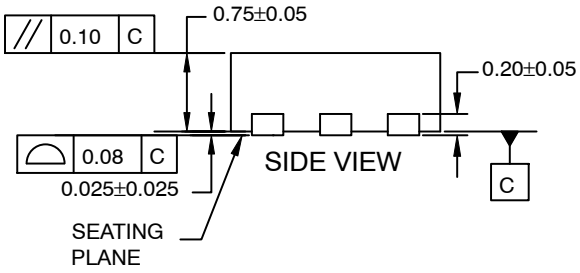
WDFN6 2x2, 0.65P
CASE 511CZ
ISSUE O

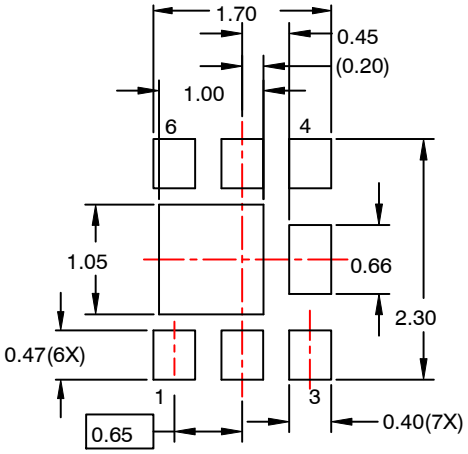
DATE 31 JUL 2016



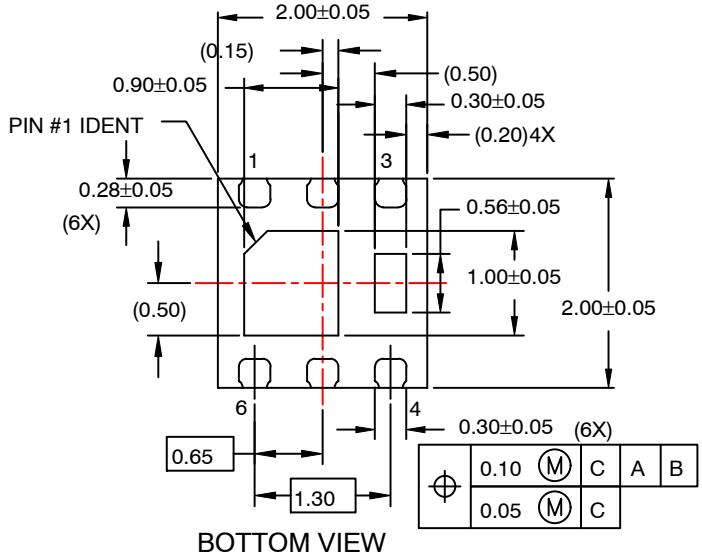


RECOMMENDED
LAND PATTERN OPT 1





RECOMMENDED
LAND PATTERN OPT 2



BOTTOM VIEW

NOTES:

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B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

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