EVALUATION KIT AVAILABLE

MAX187/MAX189

+5V, Low-Power, 12-Bit Serial ADCs

General Description

The MAX187/MAX189 serial 12-bit analog-to-digital converters (ADCs) operate from a single +5V supply and accept a 0 to 5V analog input. Both parts feature an 8.5µs successive-approximation ADC, a fast track/hold (1.5µs), an on-chip clock, and a high-speed 3-wire serial interface.

The MAX187/MAX189 digitize signals at a 75ksps throughput rate. An external clock accesses data from the interface, which communicates without external hardware to most digital signal processors and microcontrollers. The interface is compatible with SPI, QSPI™, and MICROWIRE®.

The MAX187 has an on-chip buffered reference, and the MAX189 requires an external reference. Both the MAX187 and MAX189 save space with 8-pin PDIP and 16-pin SO packages. Power consumption is 7.5mW and reduces to only 10µW in shutdown.

Excellent AC characteristics and very low power consumption combined with ease of use and small package size make these converters ideal for remote DSP and sensor applications, or for circuits where power consumption and space are crucial.

Features

- **12-Bit Resolution**
- **±½ LSB Integral Nonlinearity (MAX187A/MAX189A)**
- **Internal Track/Hold, 75kHz Sampling Rate**
- **Single +5V Operation**
- **Low Power: 2µA Shutdown Current**
  1.5mA Operating Current
- **Internal 4.096V Buffered Reference (MAX187)**
- **3-Wire Serial Interface, Compatible with SPI, QSPI, and MICROWIRE**
- **Small-Footprint 8-Pin PDIP and 16-Pin SO**

Applications

Portable Data Logging

Remote Digital Signal Processing

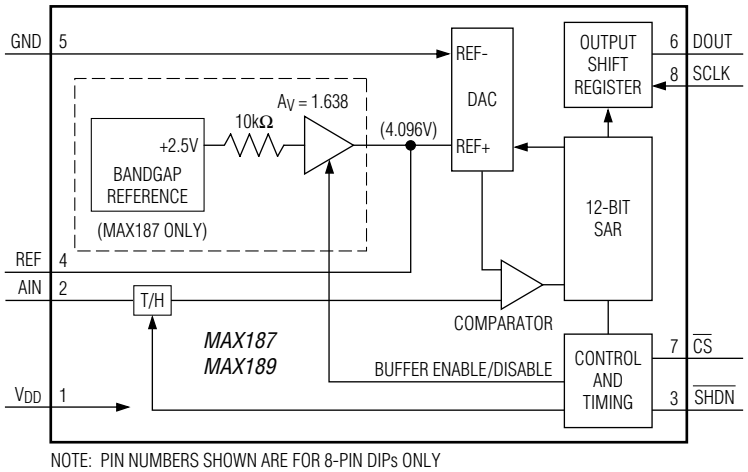
Isolated Data Acquisition

High-Accuracy Process Control

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX187.related.

Functional Diagram



NOTE: PIN NUMBERS SHOWN ARE FOR 8-PIN DIPs ONLY

QSPI is a trademark of Motorola.
MICROWIRE is a registered trademark of National Semiconductor Corp.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-0196; Rev 1; 3/12

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
AIN to GND.....-0.3V to (V_{DD} + 0.3V)
REF to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND.....-0.3V to (V_{DD} + 0.3V)
Digital Outputs to GND.....-0.3V to (V_{DD} + 0.3V)
$\overline{SHDN}$ to GND.....-0.3V to (V_{DD} + 0.3V)
REF Load Current (MAX187) .....4.0mA Continuous
REF Short-Circuit Duration (MAX187)..... ... .20s
DOUT Current.....±20mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin PDIP (derate 9.1mW/°C above +70°C).....727mW
16-Pin Wide SO (derate 14.5mW/°C above 70°C).....1157mW
Operating Temperature Ranges
MAX187_C_ _/MAX189_C_ _.....0°C to +70°C
MAX187_E_ _/MAX189_E_ _.....-40°C to +85°C
Storage Temperature Range.....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%; V_{GND} = 0V; unipolar input mode; 75ksps, f_{CLK} = 4.0MHz, external clock (50% duty cycle); MAX187—internal reference: V_{REF} = 4.096V, 4.7µF capacitor at REF pin, or MAX189—external reference: V_{REF} = 4.096V applied to REF pin, 4.7µF capacitor at REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution					12	Bits
Relative Accuracy (Note 2)		MAX18_A			±½	LSB
		MAX18_B			±1	
		MAX18_C			±2	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX18_A			±1½	LSB
		MAX18_B/C			±3	
Gain Error (Note 3)		MAX187			±3	LSB
		MAX189A			±1	
		MAX189B/C			±3	
Gain Temperature Coefficient		External reference, 4.096V		±0.8		ppm/°C
DYNAMIC SPECIFICATIONS (10kHz Sine Wave Input, 0 to 4.096V_{P-P}, 75ksps)						
Signal-to-Noise Plus Distortion Ratio	SINAD		70			dB
Total Harmonic Distortion (Up to the 5th Harmonic)	THD				-80	dB
Spurious-Free Dynamic Range	SFDR		80			dB
Small-Signal Bandwidth		Rolloff -3dB		4.5		MHz
Full-Power Bandwidth				0.8		MHz
CONVERSION RATE						
Conversion Time	t_{CONV}		5.5		8.5	µs
Track/Hold Acquisition Time	t_{ACQ}		1.5			µs
Throughput Rate		External clock, 4MHz, 13 clocks			75	ksps

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%; V_{GND} = 0V; unipolar input mode; 75ksps, f_{CLK} = 4.0MHz, external clock (50% duty cycle); MAX187—internal reference: V_{REF} = 4.096V, 4.7µF capacitor at REF pin, or MAX189—external reference: V_{REF} = 4.096V applied to REF pin, 4.7µF capacitor at REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Aperture Delay	t_{APR}				10		ns
Aperture Jitter					< 50		ps
ANALOG INPUT							
Input Voltage Range						0 to V_{REF}	V
Input Capacitance (Note 4)					16		pF
INTERNAL REFERENCE (MAX187 Only, Reference Buffer Enabled)							
REF Output Voltage	V_{REF}	T_A = +25°C		4.076	4.096	4.116	V
		T_A = T_{MIN} to T_{MAX}	MAX187_C	4.060		4.132	
			MAX187_E	4.050		4.140	
REF Short-Circuit Current						±30	mA
REF Tempco		MAX187AC/BC			±30	±50	ppm/°C
		MAX187AE/BE			±30	±60	
		MAX187C			±30		
Load Regulation (Note 5)		0 to 6mA output load			1		mV
EXTERNAL REFERENCE AT REF (Buffer Disabled, V_{REF} = 4.096V)							
Input Voltage Range				2.50		V_{DD} + 50mV	V
Input Current					200	350	µA
Input Resistance				12	20		kΩ
Shutdown REF Input Current					1.5	10	µA
DIGITAL INPUTS (SCLK, $\overline{CS}$, $\overline{SHDN}$)							
SCLK, $\overline{CS}$ Input High Voltage	V_{INH}			2.4			V
SCKL, $\overline{CS}$ Input Low Voltage	V_{INL}					0.8	V
SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}				0.15		V
SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}				±1	µA
SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 4)				15	pF
$\overline{SHDN}$ Input High Voltage	V_{INSH}			V_{DD} - 50mV			V
$\overline{SHDN}$ Input Low Voltage	V_{INSL}					0.5	V
$\overline{SHDN}$ Input Current	I_{INS}	$V_{\overline{SHDN}}$ = V_{DD} or 0V				±4.0	µA
$\overline{SHDN}$ Input Mid voltage	V_{IM}			1.5		V_{DD} - 1.5	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = Open			2.75		V
$\overline{SHDN}$ Maximum Allowed Leakage, Mid-Input		$\overline{SHDN}$ = Open		-100		100	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%; V_{GND} = 0V; unipolar input mode; 75ksps, f_{CLK} = 4.0MHz, external clock (50% duty cycle); MAX187—internal reference: V_{REF} = 4.096V, 4.7µF capacitor at REF pin, or MAX189—external reference: V_{REF} = 4.096V applied to REF pin, 4.7µF capacitor at REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL OUTPUT (DOUT)							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
		I_{SINK} = 16mA			0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA		4			V
Three-State Leakage Current	I_L	$V_{\overline{CS}}$ = 5V				±10	µA
Three-State Output Capacitance	C_{OUT}	$V_{\overline{CS}}$ = 5V (Note 4)				15	pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.75		5.25	V
Supply Current	I_{DD}	Operating mode	MAX187		1.5	2.5	mA
			MAX189		1.0	2.0	
		Power-down mode			2	10	µA
Power-Supply Rejection	PSR	V_{DD} = +5V ±5%; external reference, 4.096V; full-scale input (Note 6)			±0.06	±0.5	mV

TIMING CHARACTERISTICS

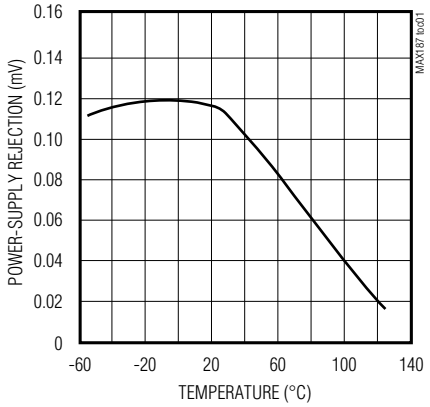
(V_{DD} = +5V ±5%, T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Track/Hold Acquisition Time	t_{ACQ}	$\overline{CS}$ = high (Note7)		1.5			µs
SCLK Fall to Output Data Valid	t_{DQ}	C_{LOAD} = 100pF	MAX18_ _C/E	20		150	ns
			MAX18_ _M	20		200	
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_{LOAD} = 100pF				100	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	C_{LOAD} = 100pF				100	ns
SCLK Clock Frequency	t_{SCLK}					5	MHz
SCLK Pulse Width High	t_{CH}			100			ns
SCLK Pulse Width Low	t_{CL}			100			ns
SCLK Low to $\overline{CS}$ Fall Setup Time	t_{CSO}			50			ns
$\overline{CS}$ Pulse Width	$t_{\overline{CS}}$			500			ns

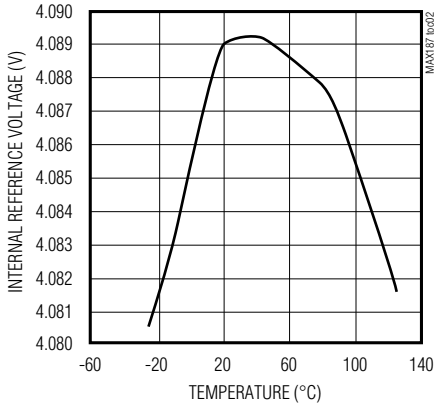
Note 1: Tested at V_{DD} = +5V.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: MAX187—internal reference, offset nulled; MAX189–external +4.096V reference, offset nulled. Excludes reference errors.
Note 4: Guaranteed by design. Not subject to production testing.
Note 5: External load should not change during conversion for specified ADC accuracy.
Note 6: DC test, measured at 4.75V and 5.25V only.
Note 7: To guarantee acquisition time, t_{ACQ} is the maximum time the device takes to acquire the signal, and is also the minimum-time needed for the signal to be acquired.

Typical Operating Characteristics

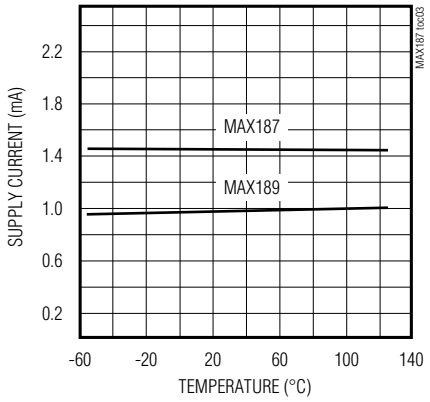
POWER-SUPPLY REJECTION vs. TEMPERATURE



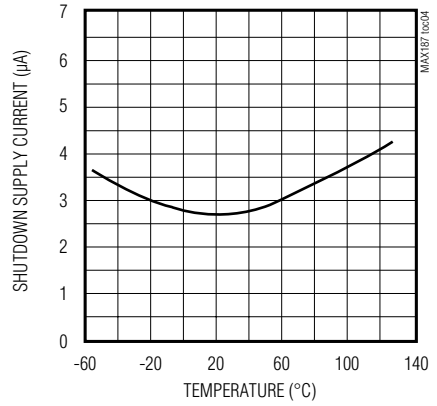
V_{REF} vs. TEMPERATURE



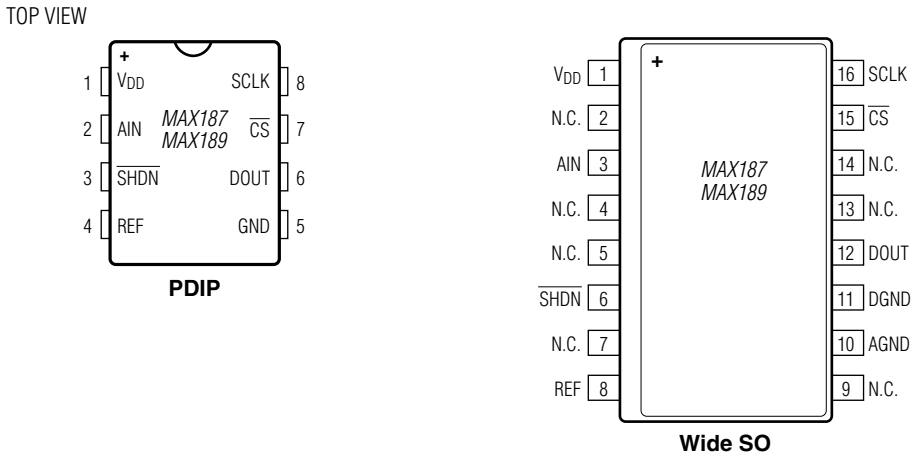
SUPPLY vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



Pin Configurations



Pin Description

PIN		NAME	FUNCTION
PDIP	WIDE SO		
1	1	V_{DD}	Supply Voltage. +5V, ±5%
2	3	AIN	Sampling Analog Input. 0V to V_{REF} range
3	6	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX187/MAX189 down to 10µA (max) supply current. Both MAX187 and MAX189 are fully operational with either $\overline{SHDN}$ high or unconnected. For the MAX187, pulling $\overline{SHDN}$ high enables the internal reference, and letting $\overline{SHDN}$ unconnected disables the internal reference and allows for the use of an external reference.
4	8	REF	Reference Voltage—sets analog voltage range and functions as a 4.096V output for the MAX187 with enabled internal reference. REF also serves as a +2.5V to V_{DD} input for a precision reference for both MAX187 (disabled internal reference) and MAX189. Bypass with 4.7µF if internal reference is used, and with 0.1µF if an external reference is applied.
5	—	GND	Analog and Digital Ground
—	10	AGND	Analog Ground
—	11	DGND	Digital Ground
6	12	DOUT	Serial Data Output. Data changes state at SCLK's falling edge.
7	15	$\overline{CS}$	Active-Low Chip Select. Initiates conversions on the falling edge. When $\overline{CS}$ is high, DOUT is high impedance.
8	16	SCLK	Serial Clock Input. Clocks data out with rates up to 5MHz.
—	2, 4, 5, 7, 9, 13. 14	N.C.	No Connection. Not internally connected. Connect to AGND for best noise performance.

Detailed Description

Converter Operation

The MAX187/MAX189 use input track/hold (T/H) and successive approximation register (SAR) circuitry to convert an analog input signal to a digital 12-bit output. No external hold capacitor is needed for the T/H. Figures 3a and 3b show the MAX187/MAX189 in their simplest configuration. The MAX187/MAX189 convert input signals in the 0V to V_{REF} range in 10µs, including T/H acquisition time. The MAX187's internal reference is trimmed to 4.096V, while the MAX189 requires an external reference. Both devices accept external reference voltages from +2.5V to V_{DD}. The serial interface requires only three digital lines, SCLK, $\overline{CS}$, and DOUT, and provides easy interface to microprocessors (µPs).

Both converters have two modes: normal and shutdown. Pulling $\overline{SHDN}$ low shuts the device down and reduces supply current to below 10µA, while pulling $\overline{SHDN}$ high or leaving it floating puts the device into the operational mode.

A conversion is initiated by $\overline{CS}$ falling. The conversion result is available at DOUT in unipolar serial format. A high bit, signaling the end of conversion (EOC), followed by the data bits (MSB first), make up the serial data stream.

The MAX187 operates in one of two states: (1) internal reference and (2) external reference. Select internal reference operation by forcing $\overline{SHDN}$ high, and external reference operation by floating $\overline{SHDN}$.

Analog Input

Figure 4 illustrates the sampling architecture of the ADC's analog comparator. The full-scale input voltage depends on the voltage at REF.

REFERENCE	ZERO SCALE	FULL SCALE
Internal Reference (MAX187 only)	0V	+4.096V
External Reference	0V	VREF

For specified accuracy, the external reference voltage range spans from +2.5V to V_{DD}.

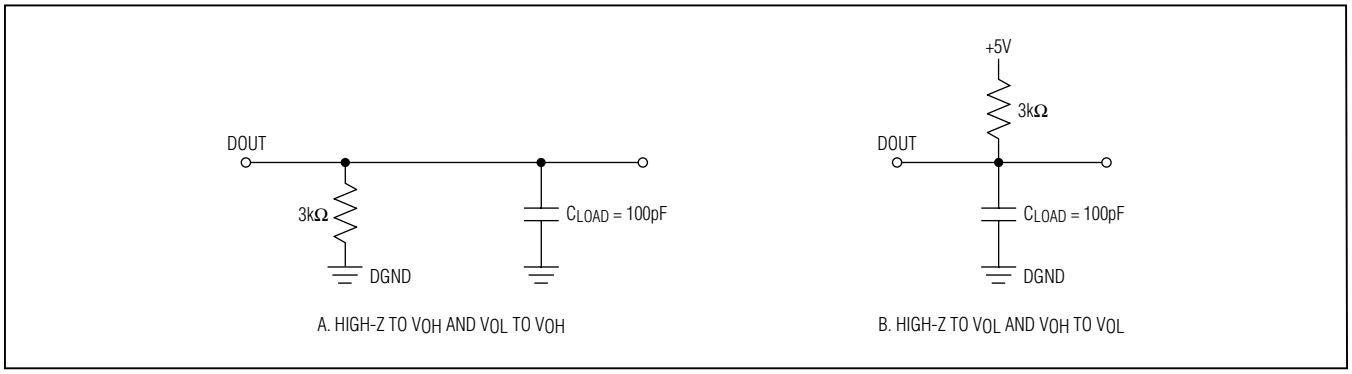


Figure 1. Load Circuits for DOUT Enable Time

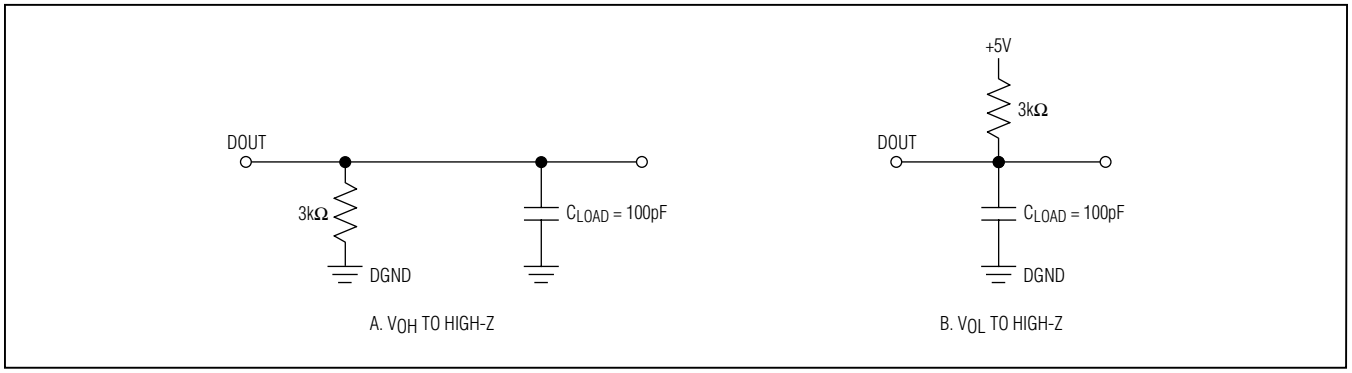


Figure 2. Load Circuits for DOUT Disable Time

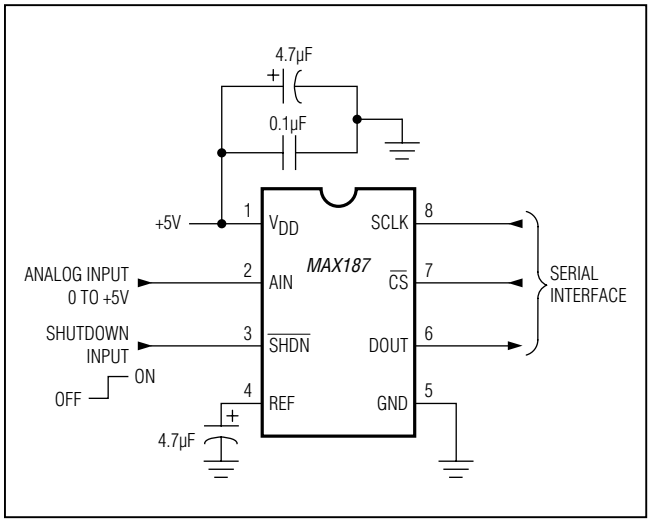


Figure 3a. MAX187 Operational Diagram

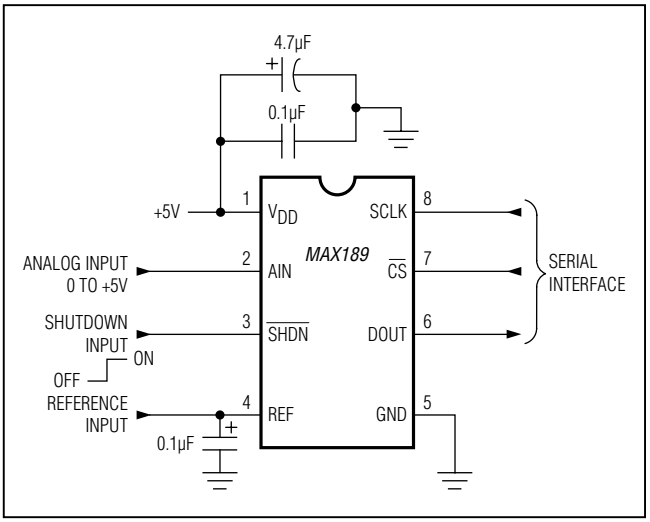


Figure 3b. MAX189 Operational Diagram

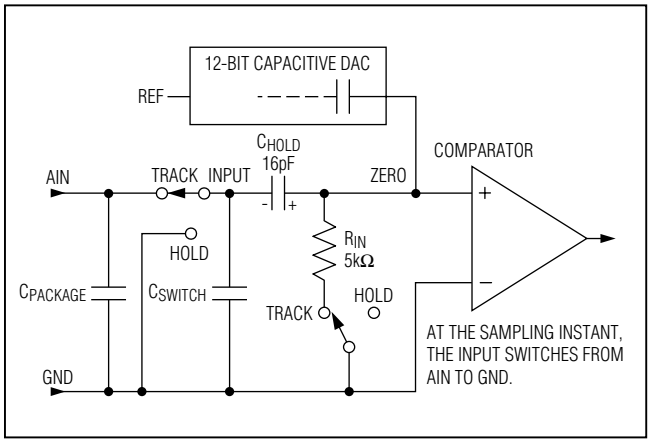


Figure 4. Equivalent Input Circuit

Track/Hold

In track mode, the analog signal is acquired and stored in the internal hold capacitor. In hold mode, the T/H switch opens and maintains a constant input to the ADC's SAR section.

During acquisition, the analog input AIN charges capacitor C_{HOLD}. Bringing $\overline{CS}$ low ends the acquisition interval. At this instant, the T/H switches the input side of C_{HOLD} to GND. The retained charge on C_{HOLD} represents a sample of the input, unbalancing the node ZERO at the comparator's input.

In hold mode, the capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of a 12-bit resolution. This action is equivalent to transferring a charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal. At the conversion's end, the input side of C_{HOLD} switches back to AIN, and C_{HOLD} charges to the input signal again.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{ACQ} = 9\ (R_S + R_{IN})\ 16pF$$

where R_{IN} = 5kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Source impedances below 5kΩ do not significantly affect the AC performance of the ADC.

Input Bandwidth

The ADCs' input tracking circuitry has a 4.5MHz small-signal bandwidth, and an 8V/µs slew rate. It is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted high-frequency signals into the frequency band of interest, an anti-alias filter is recommended. See the MAX274/MAX275 continuous-time filters data sheet.

Input Protection

Internal protection diodes that clamp the analog input allow the input to swing from GND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the input must not exceed V_{DD} by more than 50mV, or be lower than GND by 50mV.

If the analog input exceeds the supplies by more than 50mV beyond the supplies, limit the input current to 2mA, since larger currents degrade conversion accuracy.

Driving the Analog Input

The input lines to AIN and GND should be kept as short as possible to minimize noise pickup. Shield longer leads. Also see the *Input Protection* section.

Because the MAX187/MAX189 incorporate a T/H, the drive requirements of the op amp driving AIN are less stringent than those for a successive-approximation ADC without a T/H. The typical input capacitance is 16pF. The amplifier bandwidth should be sufficient to handle the frequency of the input signal. The MAX400 and OP07 work well at lower frequencies. For higher-frequency operation, the MAX427 and OP27 are practical choices. The allowed input frequency range is limited by the 75ksps sample rate of the MAX187/MAX189. Therefore, the maximum sinusoidal input frequency allowed is 37.5kHz. Higher-frequency signals cause aliasing problems unless undersampling techniques are used.

Reference

The MAX187 can be used with an internal or external reference, while the MAX189 requires an external reference.

Internal Reference

The MAX187 has an on-chip reference with a buffered temperature-compensated bandgap diode, laser-trimmed to +4.096V ±0.5%. Its output is connected to REF and also drives the internal DAC. The output can be used as a reference voltage source for other components and can source up to 0.6mA. Decouple REF with a 4.7µF capacitor. The internal reference is enabled by pulling the $\overline{SHDN}$ pin high. Letting $\overline{SHDN}$ float disables the internal reference, which allows the use of an external reference, as described in the *External Reference* section.

External Reference

The MAX189 operates with an external reference at the REF pin. To use the MAX187 with an external reference, disable the internal reference by letting $\overline{SHDN}$ float. Stay within the voltage range +2.5V to V_{DD} to achieve specified accuracy. The minimum input impedance is 12kΩ for DC currents. During conversion, the external reference must be able to deliver up to 350µA DC load current and have an output impedance of 10Ω or less. The recommended minimum value for the bypass capacitor is 0.1µF. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor.

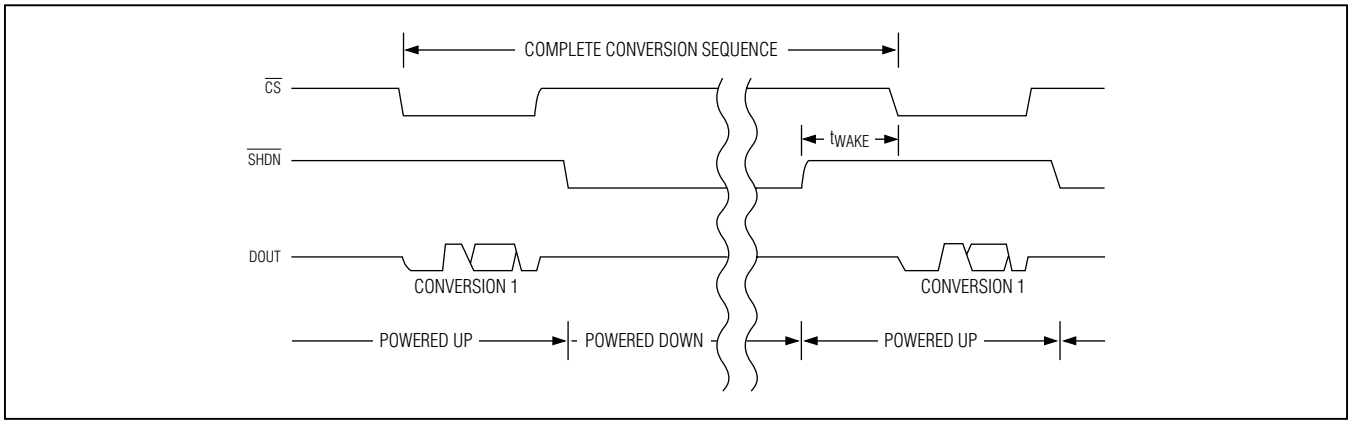


Figure 5. MAX187/MAX189 Shutdown Sequence

Serial Interface

Initialization After Power-Up and Starting a Conversion

When power is first applied, it takes the fully discharged 4.7µF reference bypass capacitor up to 20ms to provide adequate charge for specified accuracy. With $\overline{SHDN}$ not pulled low, the MAX187/MAX189 are now ready to convert.

To start a conversion, pull $\overline{CS}$ low. At $\overline{CS}$'s falling edge, the T/H enters its hold mode and a conversion is initiated. After an internally timed 8.5µs conversion period, the end of conversion is signaled by DOUT pulling high. Data can then be shifted out serially with the external clock.

Using $\overline{SHDN}$ to Reduce Supply Current

Power consumption can be reduced significantly by shutting down the MAX187/MAX189 between conversions. This is shown in Figure 6, a plot of average supply current vs. conversion rate. Because the MAX189 uses an external reference voltage (assumed to be present continuously), it "wakes up" from shutdown more quickly, and therefore provides lower average supply currents. The wakeup-time, tWAKE, is the time from $\overline{SHDN}$ deasserted to the time when a conversion may be initiated. For the MAX187, this time is 2µs. For the MAX189, this time depends on the time in shutdown (see Figure 7) because the external 4.7µF reference bypass capacitor loses charge slowly during shutdown (see the specifications for shutdown, REF Input Current = 10µA max).

External Clock

The actual conversion does not require the external clock. This frees the µP from the burden of running the SAR conversion clock, and allows the conversion result to be read back at the µP's convenience at any clock rate from 0 to 5MHz. The clock duty cycle is unrestricted if each clock phase is at least 100ns. Do not run the clock while a conversion is in progress.

Timing and Control

Conversion-start and data-read operations are controlled by the $\overline{CS}$ and SCLK digital inputs. The timing diagrams of Figures 8 and 9 outline the operation of the serial interface.

A $\overline{CS}$ falling edge initiates a conversion sequence: The T/H stage holds input voltage, the ADC begins to convert, and DOUT changes from high impedance to logic low. SCLK must be kept inactive during the conversion. An internal register stores the data when the conversion is in progress.

End of conversion (EOC) is signaled by DOUT going high. DOUT's rising edge can be used as a framing signal. SCLK shifts the data out of this register any time after the conversion is complete. DOUT transitions on SCLK's falling edge. The next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits. Since there are 12 data bits and one leading high bit, at least 13 falling clock edges are needed to shift out these bits. Extra clock pulses occurring after the conversion result has been clocked out, and prior to a rising edge of $\overline{CS}$, produce trailing 0s at DOUT and have no effect on converter operation.

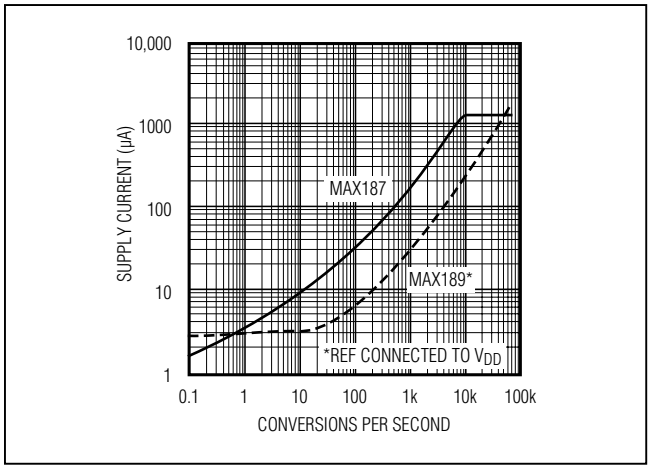


Figure 6. Average Supply Current vs. Conversion Rate

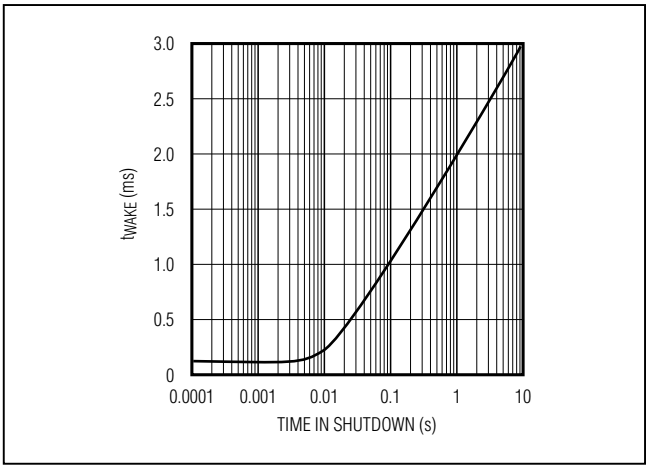


Figure 7. t_{WAKE} vs. Time in Shutdown (MAX187 Only)

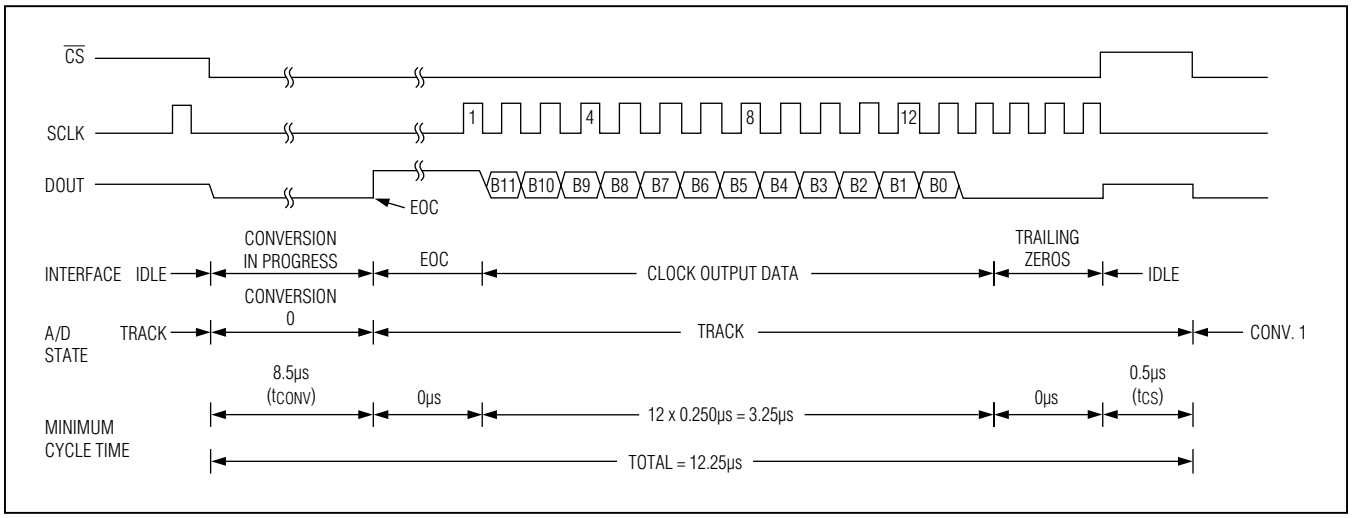


Figure 8. MAX187/MAX189 Interface Timing Sequence

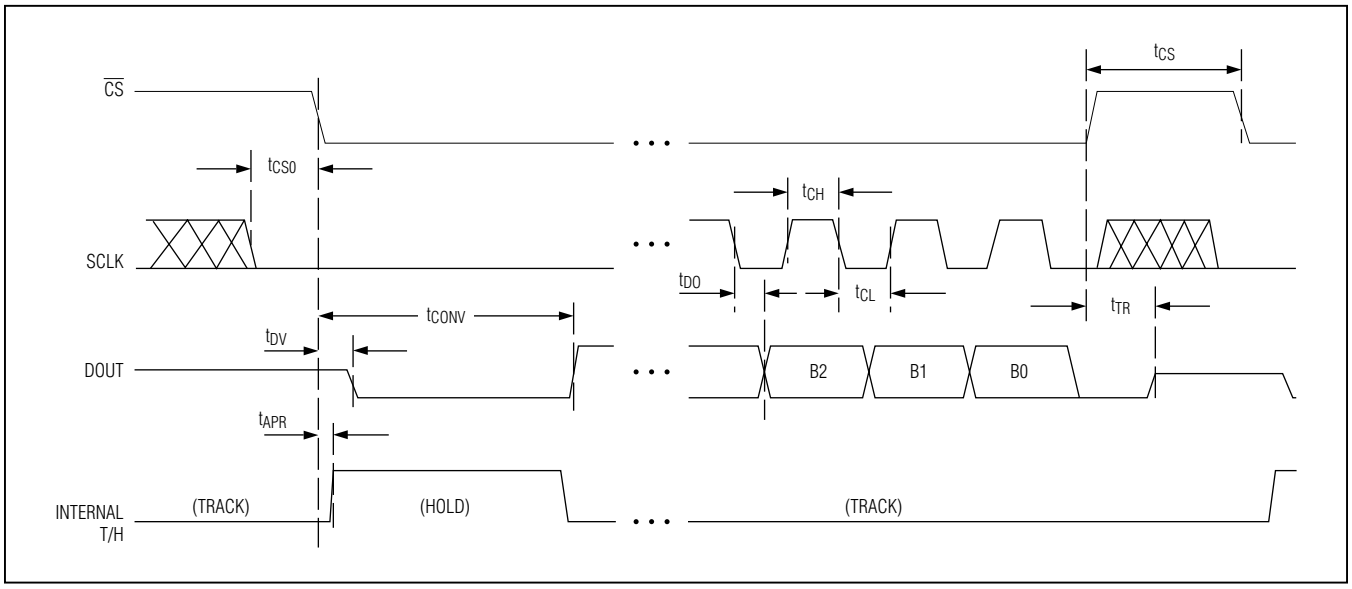


Figure 9. MAX187/MAX189 Detailed Serial-Interface Timing

Minimum cycle time is accomplished by using DOUT's rising edge as the EOC signal. Clock out the data with 13 clock cycles at full speed. Raise $\overline{CS}$ after the conversion's LSB has been read. After the specified minimum time, t_{ACQ}, $\overline{CS}$ can be pulled low again to initiate the next conversion.

Output Coding and Transfer Function

The data output from the MAX187/MAX189 is binary, and Figure 10 depicts the nominal transfer function. Code transitions occur halfway between successive integer LSB values. If V_{REF} = +4.096V, then 1 LSB = 1.00mV or 4.096V/4096.

Dynamic Performance

High-speed sampling capability and a 75ksps throughput make the MAX187/MAX189 ideal for wideband signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm that determines its spectral content. Conversion errors are then seen as spectral elements outside of the fundamental input frequency. ADCs have traditionally been evaluated by specifications such as Zero and Full-Scale Error, Integral Nonlinearity (INL), and Differential Nonlinearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal-processing applications, where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS amplitude of all other ADC output signals. The input bandwidth is limited to frequencies above DC and below one-half the ADC sample (conversion) rate.

The theoretical minimum ADC noise is caused by quantization error and is a direct result of the ADC's resolution: SINAD = (6.02N + 1.76)dB, where N is the number of bits of resolution. An ideal 12-bit ADC can, therefore, do no better than 74dB. An FFT plot of the output shows the output level in various spectral bands. Figure 11 shows the result of sampling a pure 10kHz sine wave at a 75ksps rate with the MAX187/MAX189.

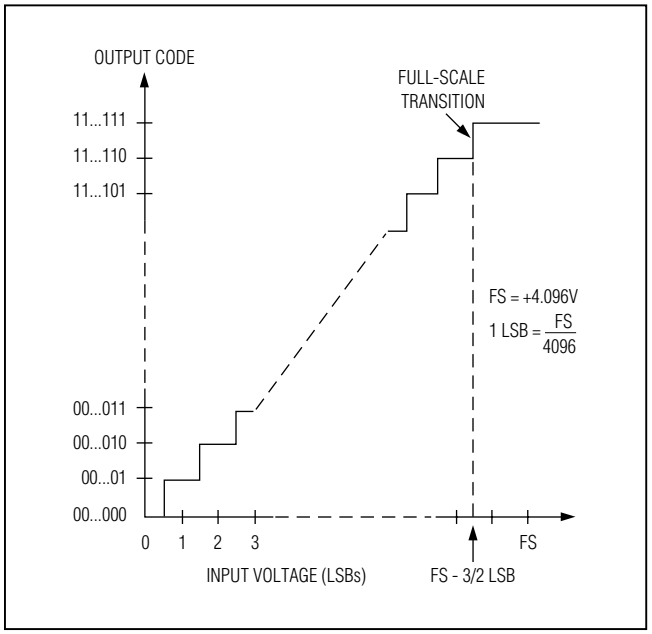


Figure 10. MAX187/MAX189 UnipolarTransfer Function, 4.096V = Full Scale

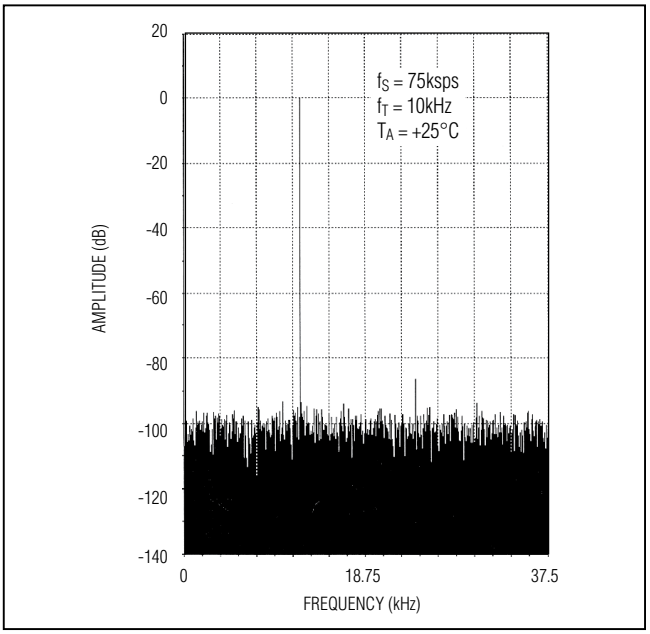


Figure 11. MAX187/MAX189 FFT plot

The effective resolution (effective number of bits) the ADC provides can be determined by transposing the above equation and substituting in the measured SINAD: N = (SINAD - 1.76)/6.02. Figure 12 shows the effective number of bits as a function of the input frequency for the MAX187/MAX189.

Total Harmonic Distortion

If a pure sine wave is sampled by an ADC at greater than the Nyquist frequency, the nonlinearities in the ADC's transfer function create harmonics of the input frequency present in the sampled output data.

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all the harmonics (in the frequency band above DC and below one-half the sample rate, but not including the DC component) to the RMS amplitude of the fundamental frequency. This is expressed as follows:

$$THD = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots V_N^2}}{V_1}$$

where V_1 is the fundamental RMS amplitude, and V_2 through V_N are the amplitudes of the 2nd through Nth harmonics. The THD specification in the *Electrical Characteristics* includes the 2nd through 5th harmonics.

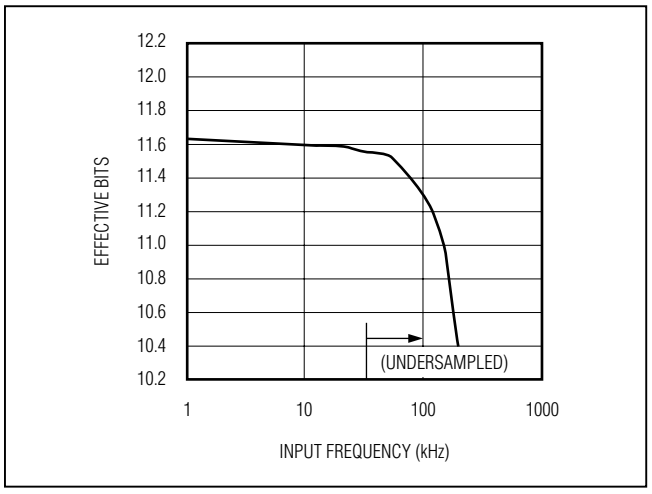


Figure 12. Effective Bits vs. Input Frequency

Applications Information

Connection to Standard Interfaces

The MAX187/MAX189 serial interface is fully compatible with SPI, QSPI, and MICROWIRE standard serial interfaces.

If a serial interface is available, set the CPU's serial interface in master mode so the CPU generates the serial clock. Choose a clock frequency up to 2.5MHz.

1) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low. Keep SCLK low.
2) Wait the for the maximum conversion time specified before activating SCLK. Alternatively, look for a DOUT rising edge to determine the end of conversion.
3) Activate SCLK for a minimum of 13 clock cycles. The first falling clock edge will produce the MSB of the DOUT conversion. DOUT output data transitions on SCLK's falling edge and is available in MSB-first format. Observe the SCLK to DOUT valid timing characteristic. Data can be clocked into the µP on SCLK's rising edge.
4) Pull $\overline{CS}$ high at or after the 13th falling clock edge. If $\overline{CS}$ remains low, trailing zeros are clocked out after the LSB.
5) With $\overline{CS}$ = high, wait the minimum specified time, t_{CS}, before launching a new conversion by pulling $\overline{CS}$ low. If a conversion is aborted by pulling $\overline{CS}$ high before the conversions end, wait for the minimum acquisition time, t_{ACQ}, before starting a new conversion.

Data can be output in 1-byte chunks or continuously, as shown in Figure 8. The bytes will contain the result of the conversion padded with one leading 1, and trailing 0s if SCLK is still active with $\overline{CS}$ kept low.

SPI and MICROWIRE

When using SPI or QSPI, set CPOL = 0 and CPHA = 0. Conversion begins with a $\overline{CS}$ falling edge. DOUT goes low, indicating a conversion in progress. Wait until DOUT goes high or the maximum specified 8.5µs conversion time. Two consecutive 1-byte reads are required to get the full 12 bits from the ADC. DOUT output data transitions on SCLK's falling edge and is clocked into the µP on SCLK's rising edge.

The first byte contains a leading 1 and 7 bits of conversion result. The second byte contains the remaining 5 bits and 3 trailing 0s. See Figure 13 for connections and Figure 14 for timing.

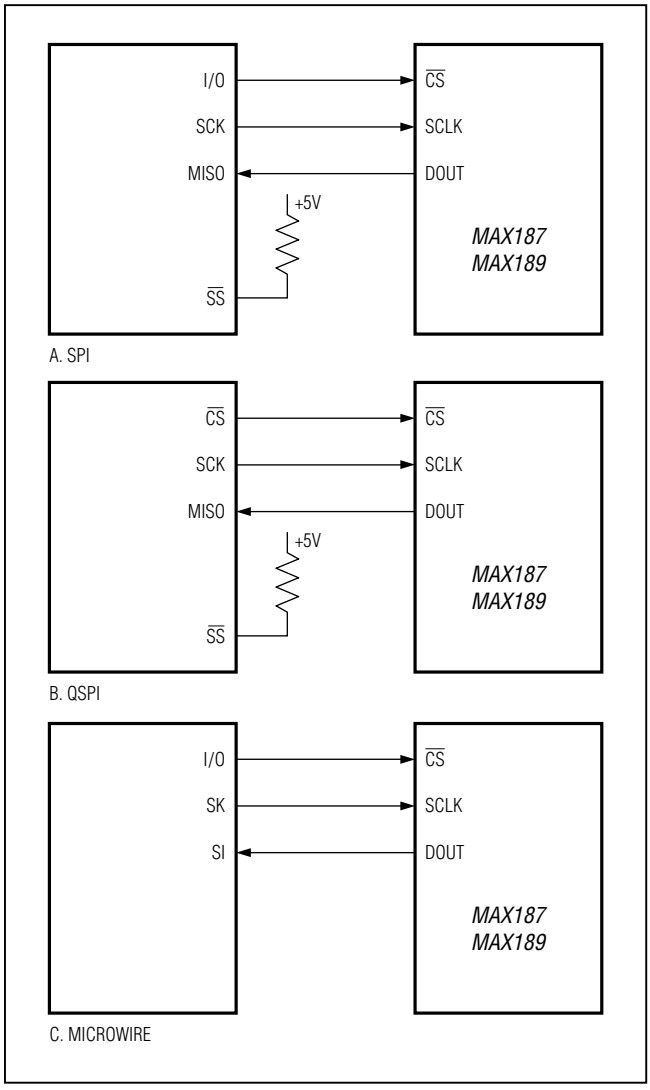


Figure 13. Common Serial-Interface Connections to the MAX187/MAX189

QSPI

Set CPOL = CPHA = 0. Unlike SPI, which requires two 1-byte reads to acquire the 12 bits of data from the ADC, QSPI allows the minimum number of clock cycles necessary to clock in the data. The MAX187/MAX189 require 13 clock cycles from the µP to clock out the 12 bits of data with no trailing 0s (Figure 15). The maximum clock frequency to ensure compatibility with QSPI is 2.77MHz.

Opto-Isolated Interface, Serial-to-Parallel Conversion

Many industrial applications require electrical isolation to separate the control electronics from hazardous electrical conditions, provide noise immunity, or prevent excessive current flow where ground disparities exist between the ADC and the rest of the system. Isolation amplifiers typically used to accomplish these tasks are expensive. In cases where the signal is eventually converted to a digital form, it is cost effective to isolate the input using opto-couplers in a serial link.

The MAX187 is ideal in this application because it includes both T/H amplifier and voltage reference, operates from a single supply, and consumes very little power (Figure 16).

The ADC results are transmitted across a 1500V isolation barrier provided by three 6N136 opto-isolators. Isolated power must be supplied to the converter and the isolated side of the opto-couplers. 74HC595 three-state shift registers are used to construct a 12-bit parallel data output. The timing sequence is identical to the timing shown in Figure 8. Conversion speed is limited by the delay through the opto-isolators. With a 140kHz clock, conversion time is 100µs.

The universal 12-bit parallel data output can also be used without the isolation stage when a parallel interface is required. Clock frequencies up to 2.9MHz are possible without violating the 20ns shift-register setup time. Delay or invert the clock signal to the shift registers beyond 2.9MHz.

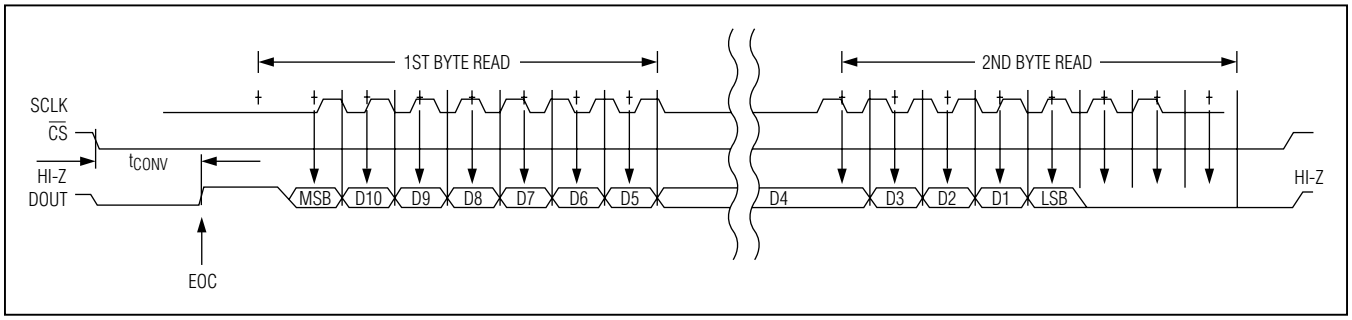


Figure 14. SPI/MICROWIRE Serial Interface Timing (CPOL = CPHA = 0)

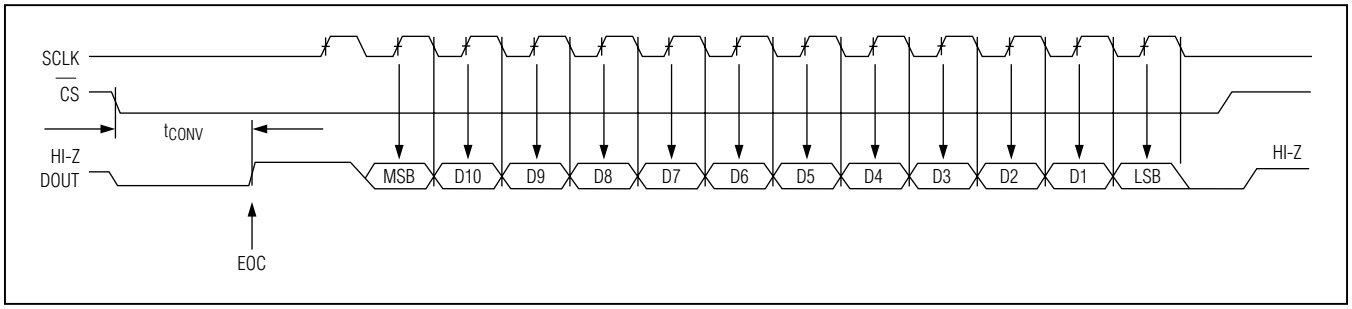


Figure 15. QSPI Serial Interface Timing (CPOL = CPHA = 0)

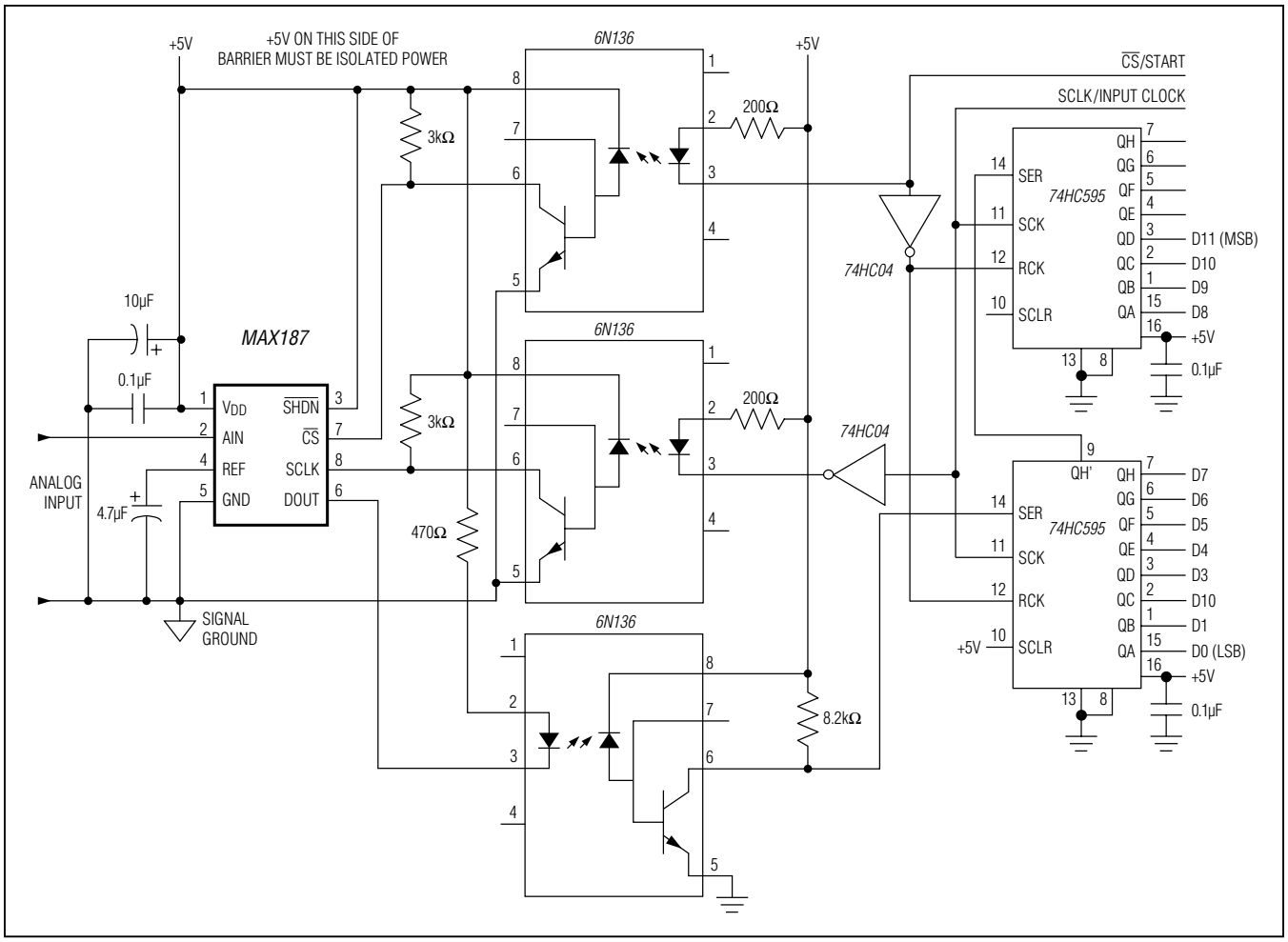


Figure 16. 12-Bit Isolated ADC

Layout, Grounding, Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 17 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at GND, separate from the logic ground. All other analog grounds should be connected to this ground. The 16-pin versions also have a dedicated DGND pin available. Connect DGND to this star ground point for further noise reduction. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the ADC's high-speed comparator. Bypass this supply to the single-point analog ground with 0.01µF and 4.7µF bypass capacitors. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter to attenuate supply noise (Figure 17).

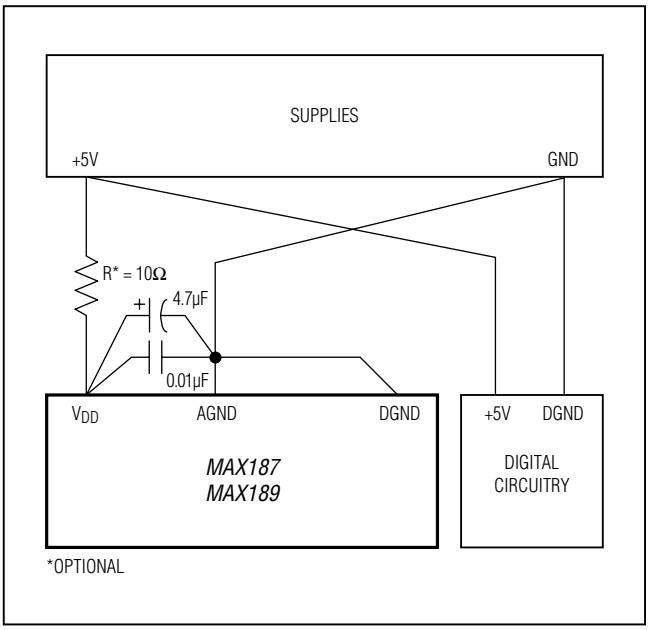


Figure 17. Power-Supply Grounding Condition

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	ERROR (LSB)
MAX187ACPA+	0°C to +70°C	8 PDIP	±1/2
MAX187BCPA+	0°C to +70°C	8 PDIP	±1
MAX187CCPA+	0°C to +70°C	8 PDIP	±2
MAX187ACWE+	0°C to +70°C	16 Wide SO	±1/2
MAX187BCWE+	0°C to +70°C	16 Wide SO	±1
MAX187CCWE+	0°C to +70°C	16 Wide SO	±2
MAX187AEPA+	-40°C to +85°C	8 PDIP	±1/2
MAX187BEPA+	-40°C to +85°C	8 PDIP	±1
MAX187CEPA+	-40°C to +85°C	8 PDIP	±2
MAX187AEWE+	-40°C to +85°C	16 Wide SO	±1/2
MAX187BEWE+	-40°C to +85°C	16 Wide SO	±1
MAX187CEWE+	-40°C to +85°C	16 Wide SO	±2
MAX189ACPA+	0°C to +70°C	8 PDIP	±1/2
MAX189BCPA+	0°C to +70°C	8 PDIP	±1
MAX189CCPA+	0°C to +70°C	8 PDIP	±2
MAX189ACWE+	0°C to +70°C	16 Wide SO	±1/2
MAX189BCWE+	0°C to +70°C	16 Wide SO	±1
MAX189CCWE+	0°C to +70°C	16 Wide SO	±2
MAX189AEPA+	-40°C to +85°C	8 PDIP	±1/2
MAX189BEPA+	-40°C to +85°C	8 PDIP	±1
MAX189CEPA+	-40°C to +85°C	8 PDIP	±2
MAX189AEWE+	-40°C to +85°C	16 Wide SO	±1/2
MAX189BEWE+	-40°C to +85°C	16 Wide SO	±1
MAX189CEWE+	-40°C to +85°C	16 Wide SO	±2

+Denotes a lead(Pb)–free/RoHS–compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 PDIP	P8+3	21-0043	—
16 SO	W16+3	21-0042	90-0107

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/93	Initial release	—
1	3/12	Updated the *Electrical Characteristics* and *Ordering Information*.	1, 3, 18

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