Voltage Detectors

Voltage Detector ICs with Watchdog Timer

BD37Axx Series BD87Axx Series BD99A41F

General Description

The BD37A19FVM, BD37A41FVM, BD87A28FVM, BD87A29FVM, BD87A34FVM, BD87A41FVM and BD99A41F are watchdog timer reset ICs. It delivers a high precision detection voltage of ±1.5% and a super-low current consumption of 5 µA (Typ). It can be used in a wide range of electronic devices to monitor power supply voltages and in system operation to prevent runaway operation.

Features

- Built-in Watchdog Timer
- Reset delay time can be set with the CT pin's external capacitance
- Watchdog timer monitor time and reset time can be set with the CTW pin's external capacitance.
- Output Circuit Type: N-Channel Open Drain

Applications

All devices using microcontrollers or DSP, including vehicle equipment, displays, servers, DVD players, and telephone systems

Key Specifications

- RESET Power Supply Voltage Range: 1.0V to 10V
- WDT Power Supply Voltage Range: 2.5V to 10V
- High Precision Detection Voltage:
  (Ta = 25°C) ±1.5%
  (Ta = −40°C to 105°C) ±2.5%
- Super-Low Current Consumption: 5µA(Typ)
- Operating Temperature Range: -40°C to +105°C

Packages

W (Typ) x D (Typ) x H (Max)

- MSOP8 2.90mm x 4.00mm x 0.90mm



- SOP8 5.00mm x 6.20mm x 1.71mm



Ordering Information

B D 3 7 A 1 9 F V M - T R

Part Number	Detection Voltage	Package	Packaging and forming specification
37A : WDT H Active 87A : WDT L Active 99A : WDT H Active	19 : 1.9V 28 : 2.8V 29 : 2.9V 34 : 3.4V 41 : 4.1V	FVM : MSOP8 F : SOP8	TR: Embossed tape and reel E2: Embossed tape and reel

Lineup

Detection voltage (Typ)	INH logic	Package		Orderable Part Number
1.9V	H: Active	MSOP8	Reel of 3000	BD37A19FVM-TR
4.1V	H: Active	MSOP8	Reel of 3000	BD37A41FVM-TR
2.8V	L: Active	MSOP8	Reel of 3000	BD87A28FVM-TR
2.9V	L: Active	MSOP8	Reel of 3000	BD87A29FVM-TR
3.4V	L: Active	MSOP8	Reel of 3000	BD87A34FVM-TR
4.1V	L: Active	MSOP8	Reel of 3000	BD87A41FVM-TR
4.1V	H: Active	SOP8	Reel of 2500	BD99A41F-E2

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Pin Configurations

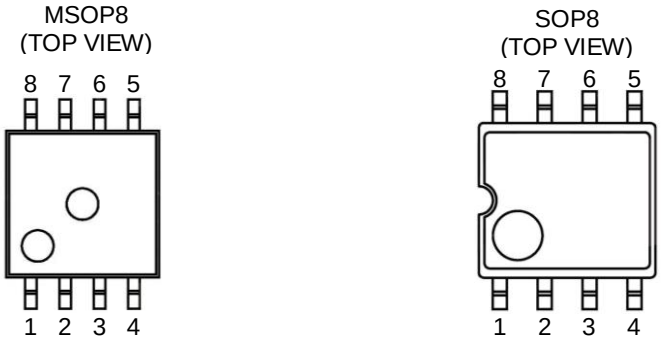


Figure 1. Pin Configurations

Pin Descriptions

BD37AxxFVM

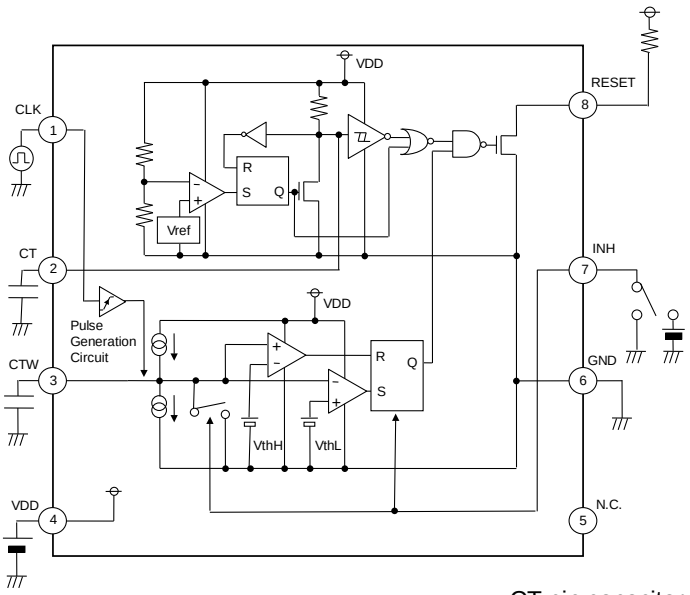
No.	Pin name	Function
1	CLK	Clock input from microcontroller
2	CT	Reset delay time setting capacitor connection pin
3	CTW	WDT time setting capacitor connection pin
4	VDD	Power supply pin
5	N.C.	NC pin
6	GND	GND pin
7	INH	WDT ON/OFF setting pin INH=H/L:WDT=ON/OFF
8	RESET	Reset output pin

BD87AxxFVM / BD99A41F

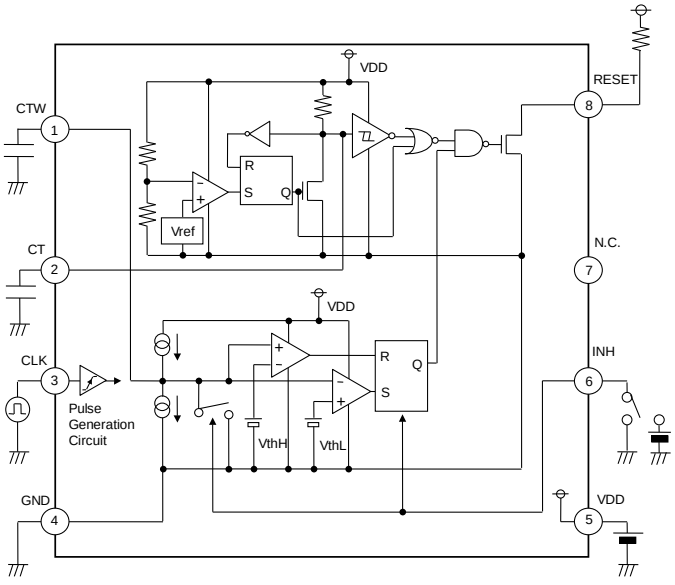
No.	Pin name	Function
1	CTW	WDT time setting capacitor connection pin
2	CT	Reset delay time setting capacitor connection pin
3	CLK	Clock input from microcontroller
4	GND	GND pin
5	VDD	Power supply pin
6	INH	WDT ON/OFF setting pin INH=H/L:WDT=OFF/ON(BD87AxxFVM) INH=H/L:WDT=ON/OFF(BD99A41F)
7	N.C.	NC pin
8	RESET	Reset output pin

Block Diagrams

BD37AxxFVM



BD87AxxFVM / BD99A41F



CT pin capacitor: 470pF to 3.3µF
CTW pin capacitor: 0.001µF to 10µF

Figure 2.Block Diagrams

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Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Power Supply Voltage *1	V_{DD}	−0.3 to 10	V
CT Pin Voltage	V_{CT}	−0.3 to V_{DD} + 0.3	V
CTW Pin Voltage	V_{CTW}	−0.3 to V_{DD} + 0.3	V
RESET Pin Voltage	V_{RESET}	−0.3 to V_{DD} + 0.3	V
INH Pin Voltage	V_{INH}	−0.3 to V_{DD} + 0.3	V
CLK Pin Voltage	V_{CLK}	−0.3 to V_{DD} + 0.3	V
Power Dissipation	Pd	0.47*2	W
		0.55*3	
Operating Ambient Temperature	Topr	−40 to + 105	°C
Storage Temperature	Tstg	−55 to + 125	°C
Maximum Junction Temperature	Tjmax	125	°C

*1 Do not exceed Pd.
*2 MSOP8 : Reduced by 4.70 mW/℃ over 25°C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).
*3 SOP8 : Reduced by 5.50 mW/℃ over 25°C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Ratings(Ta = −40°C to 105°C)

Parameter	Symbol	Min	Max	Unit
RESET Power Supply Voltage	$V_{DD\ RESET}$	1.0	10	V
WDT Power Supply Voltage	$V_{DD\ WDT}$	2.5	10	V

Electrical Characteristics

(Unless otherwise specified, Ta = −40°C to 105°C, V_{DD} = 5V)

Parameter		Symbol	Limits			Unit	Conditions
			Min	Typ	Max		
[Overall]							
Total Supply Current 1 (during WDT operation)		I_{DD1}	—	5	14	μA	INH : WDT ON Logic Input CTW = 0.1μF
Total Supply Current 2 (when WDT stopped)		I_{DD2}	—	5	14	μA	INH : WDT OFF Logic Input
Output Leak Current		I_{leak}	—	—	1	μA	V_{DD} = V_{DS} = 10V
Output Current Capacity		I_{OL}	0.7	—	—	mA	V_{DD} = 1.2V, V_{DS} = 0.5V
[RESET]							
Detection Voltage 1	1.9V Detect	V_{DET1}	1.871	1.900	1.929	V	Ta = 25°C
	2.8V Detect	V_{DET1}	2.758	2.800	2.842	V	Ta = 25°C
	2.9V Detect	V_{DET1}	2.886	2.930	2.974	V	Ta = 25°C
	3.4V Detect	V_{DET1}	3.349	3.400	3.451	V	Ta = 25°C
	4.1V Detect	V_{DET1}	4.039	4.100	4.162	V	Ta = 25°C
Detection Voltage 2	1.9V Detect	V_{DET2}	1.852	1.900	1.948	V	Ta = −40°C to 105°C
	2.8V Detect	V_{DET2}	2.730	2.800	2.870	V	Ta = −40°C to 105°C
	2.9V Detect	V_{DET2}	2.857	2.930	3.003	V	Ta = −40°C to 105°C
	3.4V Detect	V_{DET2}	3.315	3.400	3.485	V	Ta = −40°C to 105°C
	4.1V Detect	V_{DET2}	4.007	4.100	4.202	V	Ta = −40°C to 105°C
Hysteresis Width	1.9V Detect	Vrhys	V_{DET}×0.03	V_{DET}×0.13	V_{DET}×0.19	V	Ta=−40°C to 105°C
	2.8V Detect	Vrhys	V_{DET}×0.018	V_{DET}×0.045	V_{DET}×0.060	V	Ta=−40°C to 105°C
	2.9V Detect	Vrhys	V_{DET}×0.02	V_{DET}×0.05	V_{DET}×0.06	V	Ta=−40°C to 105°C
	3.4V Detect	Vrhys	V_{DET}×0.02	V_{DET}×0.05	V_{DET}×0.07	V	Ta=−40°C to 105°C
	4.1V Detect	Vrhys	V_{DET}×0.018	V_{DET}×0.035	V_{DET}×0.050	V	Ta=−40°C to 105°C

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●Electrical Characteristics - continued

(Unless otherwise specified, Ta = −40°C to 105°C, V_{DD} = 5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
RESET Transmission Delay Time: Low → High	t_{PLH}	3.9	6.9	10.1	ms	C_{CT} = 0.001µF *1 When V_{DD} = V_{DET} ±0.5V
Delay Circuit Resistance	Rrst	5.8	10.0	14.5	MΩ	V_{CT} = GND
Delay Pin Threshold Voltage	V_{CTH}	V_{DD}×0.3	V_{DD}×0.45	V_{DD}×0.6	V	R_L = 470KΩ
Delay Pin Output Current	I_{CT}	150	—	—	µA	V_{DD} = 1.50V, V_{CT} = 0.5V
Min Operating Voltage	V_{OPL}	1.0	—	—	V	V_{OL} ≤ 0.4V, R_L = 470KΩ
[WDT]						
WDT Monitor Time	t_{wH}	7.0	10.0	20.0	ms	C_{CTW} = 0.01µF *2
WDT Reset Time	t_{wL}	2.4	3.3	7.0	ms	C_{CTW} = 0.01µF *3
Clock Input Pulse Width	t_{WCLK}	500	—	—	ns	
CLK High Threshold Voltage	V_{CLKH}	V_{DD} × 0.8	—	V_{DD}	V	
CLK Low Threshold Voltage	V_{CLKL}	0	—	V_{DD} × 0.3	V	
INH High Threshold Voltage	V_{INHH}	V_{DD} × 0.8	—	V_{DD}	V	
INH Low Threshold Voltage	V_{INHL}	0	—	V_{DD} × 0.3	V	
CTW Charge Current	I_{CTWC}	0.25	0.50	0.75	µA	V_{CTW} = 0.2V
CTW Discharge Current	I_{CTWO}	0.75	1.50	2.00	µA	V_{CTW} = 0.8V

*1 t_{PLH} can be varied by changing the CT capacitance value.
t_{PLH} (s) ≈ 0.69 × Rrst (MΩ) × C_{CT} (µF) Rrst = 10 MΩ (Typ)

*2 t_{wH} can be varied by changing the CTW capacitance value.
t_{wH} (s) ≈ (0.5 × C_{CTW} (µF))/I_{CTWC} (µA) I_{CTWC} = 0.5 µA(Typ)

*3 t_{wL} can be varied by changing the CTW capacitance value.
t_{wL} (s) ≈ (0.5 × C_{CTW} (µF))/I_{CTWO} (µA) I_{CTWO} = 1.5 µA(Typ)

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Typical Performance Curves

(Unless otherwise specified, Ta = 25°C) : 4.1V Detection

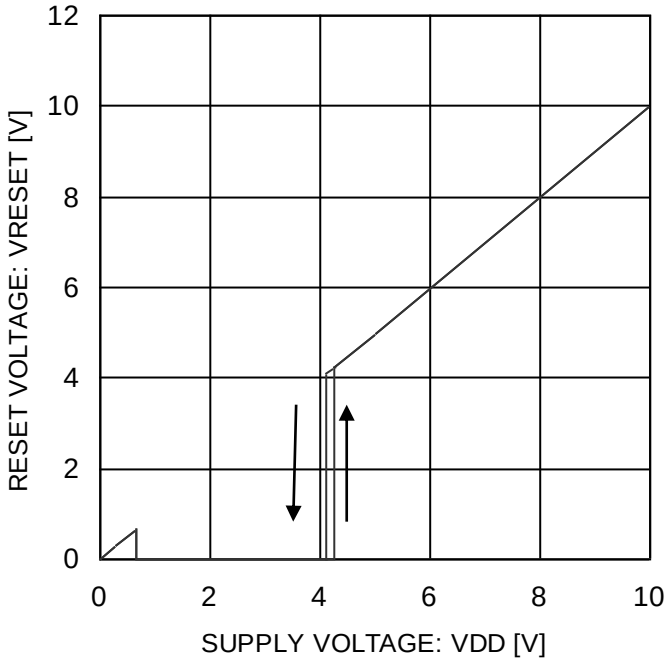


Figure 3. Detection Voltage

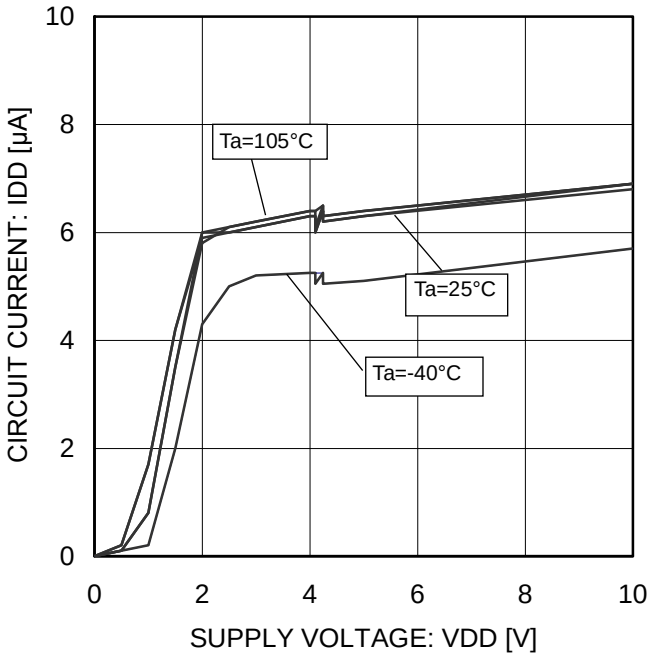


Figure 4. Total Supply Current

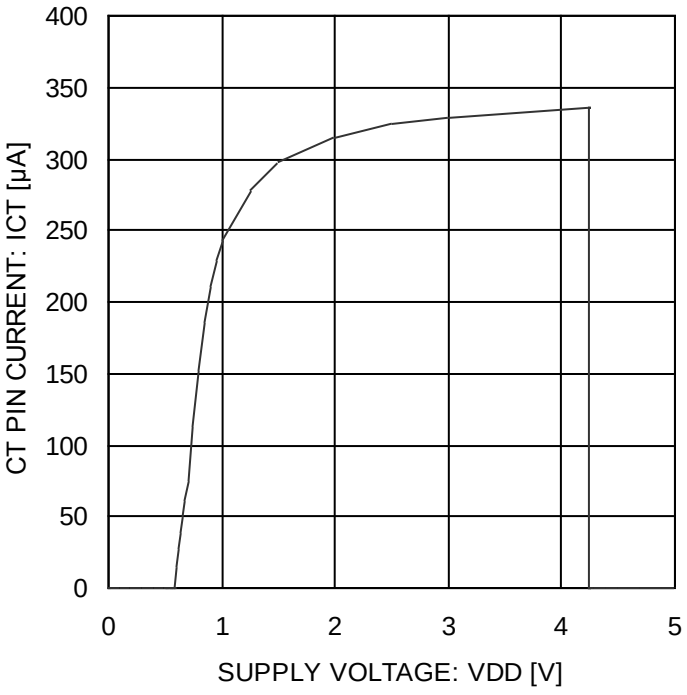


Figure 5. Delay Pin Current vs Power Supply Voltage

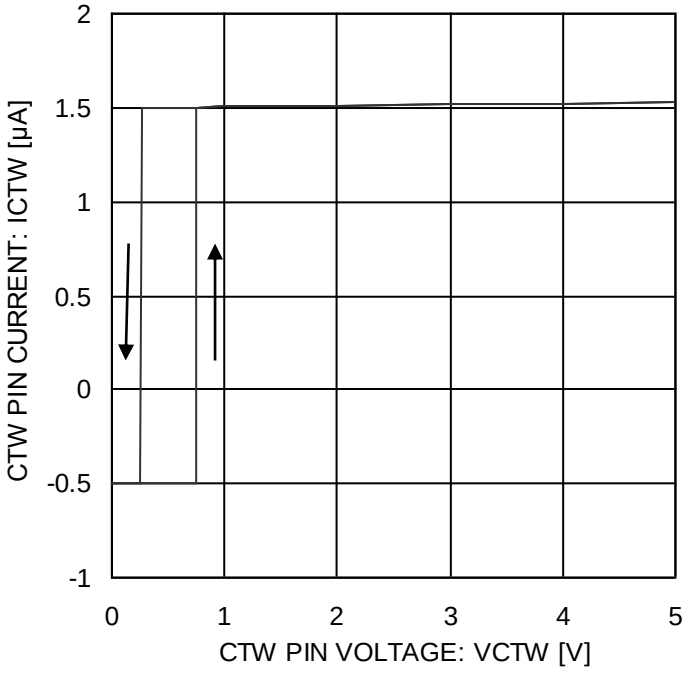


Figure 6. CTW Charge Discharge Current

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Typical Performance Curves – continued

(Unless otherwise specified, Ta = 25°C) : 4.1V Detection

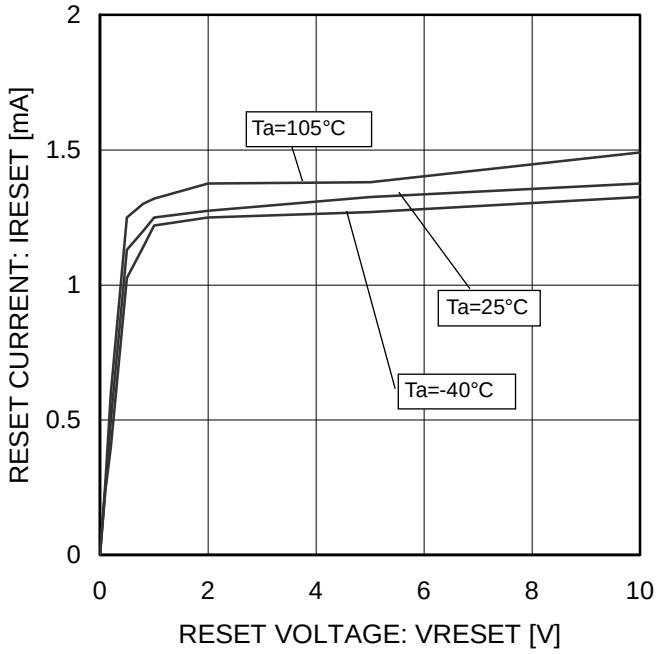


Figure 7. Output Current

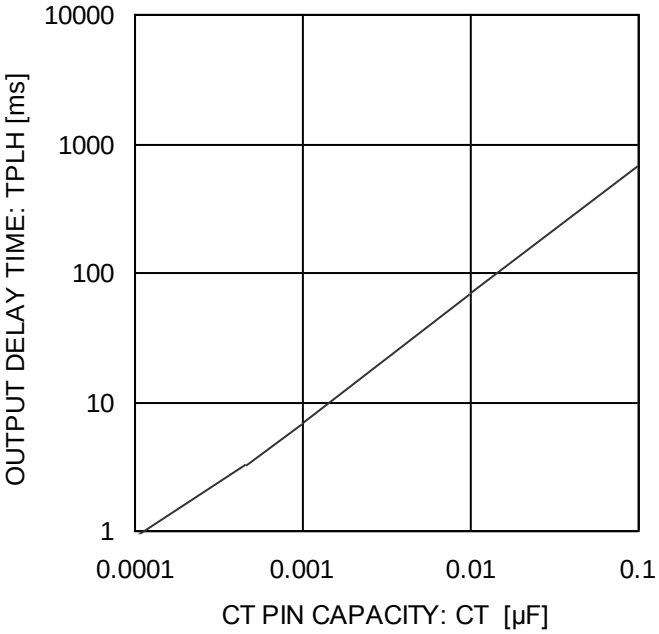


Figure 8. T RESET Transmission Delay Time vs Capacitance

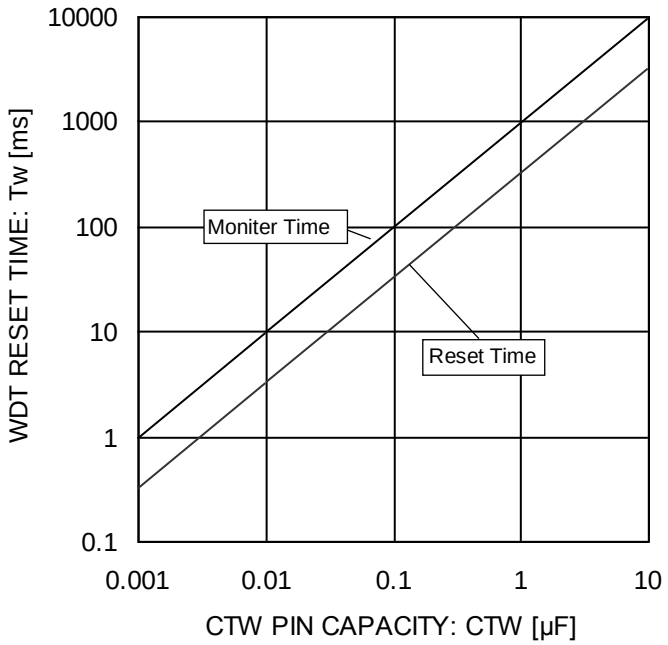


Figure 9. WDT Time vs Capacitance

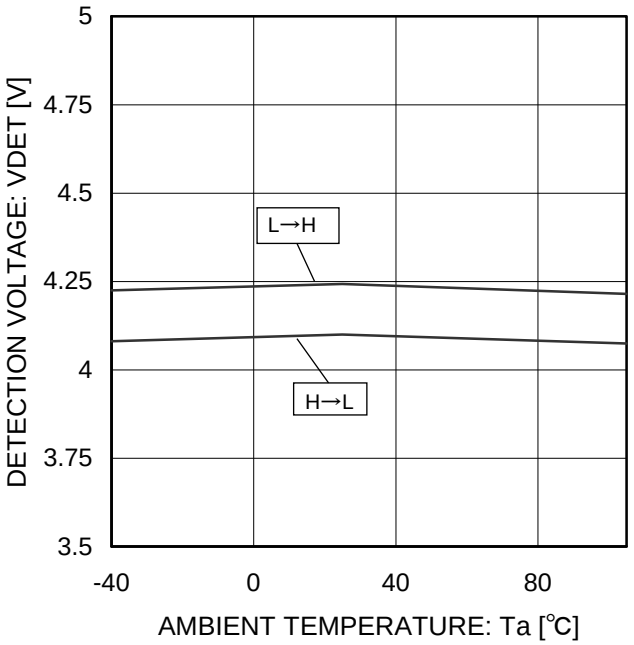


Figure 10. Detection Voltage vs Temperature

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Typical Performance Curves – continued
(Unless otherwise specified, Ta = 25°C) : 4.1V Detection

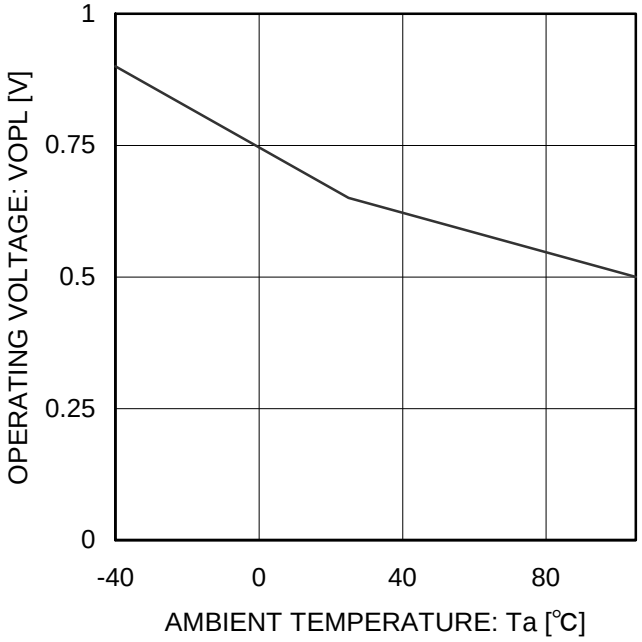


Figure 11. Operating Marginal Voltage vs Temperature

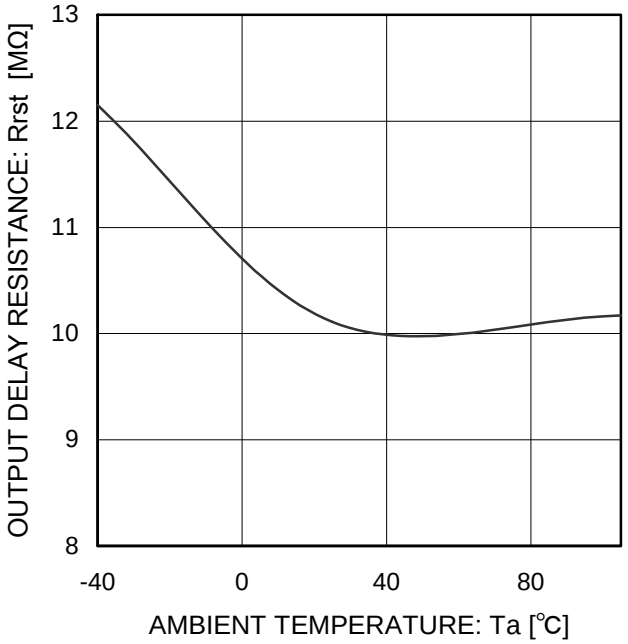


Figure 12. CT Pin Circuit Resistance vs Temperature

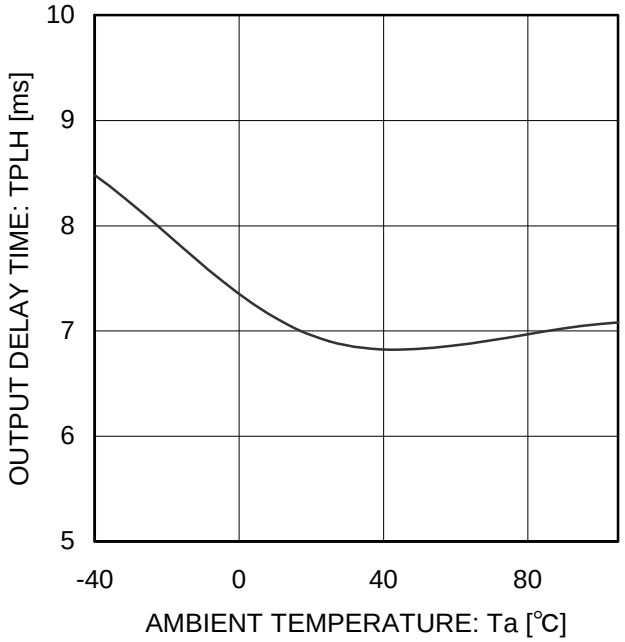


Figure 13. RESET Transmission Delay Time vs Temperature

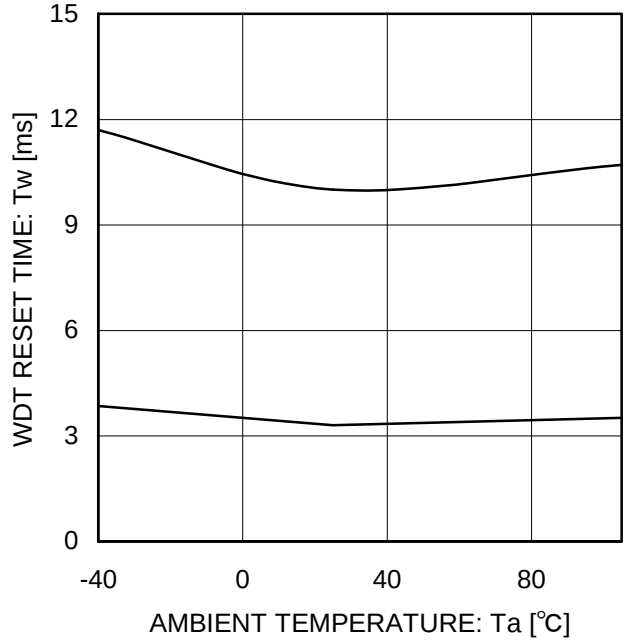


Figure 14. WDT Time vs Temperature

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Timing Chart

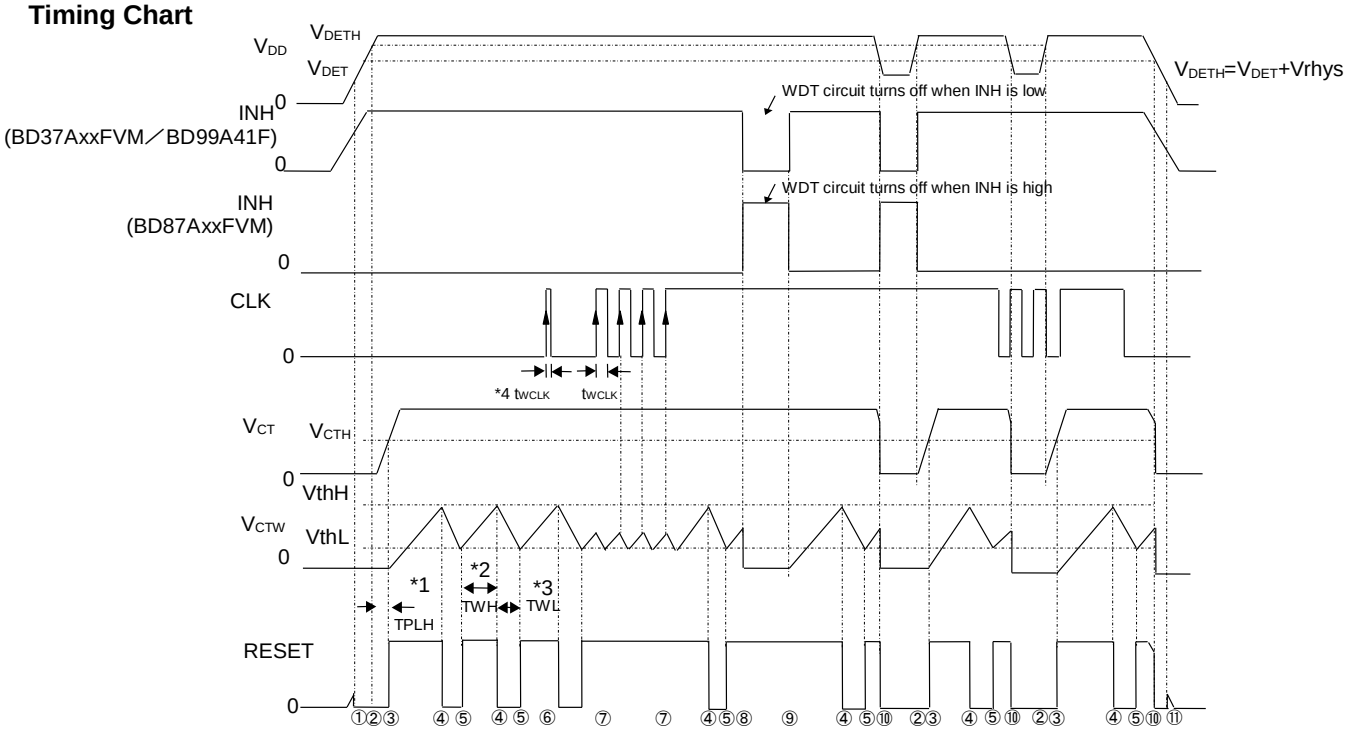


Figure 15. Timing Chart

Explanation

① The RESET pin voltage (RESET) switches to low when the power supply voltage (V_{DD}) falls to 0.8 V.

② The external capacitor connected to the CT pin begins to charge when VDD rises above the reset detection voltage (V_{DETH}). The RESET signal stays low until VDD reaches the V_{DETH} voltage and switches to high when VDD reaches or exceeds the V_{DETH} voltage. The RESET transmission delay time t_{PLH} allowed to elapse before RESET switches from low to high is given by the following equation:

$$t_{PLH}\ (s) \approx 0.69 \times Rrst(M\Omega) \times C_{CT}\ (\mu F) \cdot\cdot [1]$$

Rrst denotes the IC's built-in resistance and is designed to be 10 MΩ (Typ). C_{CT} denotes the external capacitor connected to the CT pin.

③ The external capacitor connected to the CTW pin begins to charge when RESET rises, triggering the watchdog timer.

④ The CTW pin state switches from charge to discharge when the CTW pin voltage (V_{CTW}) reaches VthH, and RESET switches from high to low. The watchdog timer monitor time t_{WH} is given by the following equation:

$$t_{WH}\ (s) \approx (0.5 \times C_{CTW}\ (\mu F))/(I_{CTWC}(\mu A)) \cdot\cdot [2]$$

I_{CTWC} denotes the CTW charge current and is designed to be 0.50 µA (Typ). C_{CTW} denotes the external capacitor connected to the CTW pin.

⑤ The CTW pin state switches from charge to discharge when V_{CTW} reaches VthL, and RESET switches from low to high. The watchdog timer reset time t_{WL} is given by the following equation:

$$t_{WL}\ (s) \approx (0.5 \times C_{CTW}\ (\mu F))/(I_{CTWO}(\mu A)) \cdot\cdot [3]$$

I_{CTWO} denotes the CTW discharge current and is designed to be 1.50 µA (Typ).

⑥ The CTW pin state may not switch from charge to discharge when the CLK input pulse width t_{WCLK} is short. Use a t_{WCLK} input pulse width of at least 500 ns.

$$t_{WCLK} \geq 500\ ns\ (Min) \cdot\cdot [4]$$

⑦ When a pulse (positive edge trigger) of at least 500 ns is input to the CLK pin while the CTW pin is charging, the CTW state switches from charge to discharge. Once it discharges to VthL, it will charge again.

⑧ Watchdog timer operation is forced off when the INH pin switches to low (L: BD37Axx Series. BD99A41F, H: BD87AxxSeries). At that time, only the watchdog timer is turned off. Reset detection is performed normally.

⑨ The watchdog timer function turns on when the INH pin switches to high(H: BD37Axx Series. BD99A41F, L: BD87AxxSeries). The external capacitor connected to the CTW pin begins to charge at that time.

⑩ RESET switches from high to low when VDD falls to the RESET detection voltage (V_{DET}) or lower.

⑪ When VDD falls to 0 V, the RESET signal stays low until VDD reaches 0.8 V.

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Power Dissipation

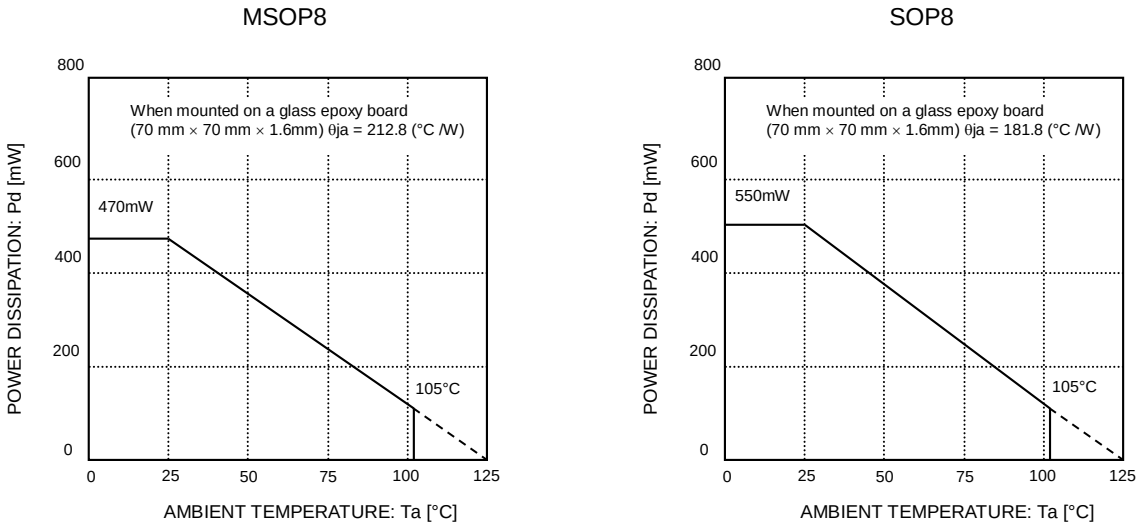


Figure 16. Power Dissipation

I/O Equivalence Circuit

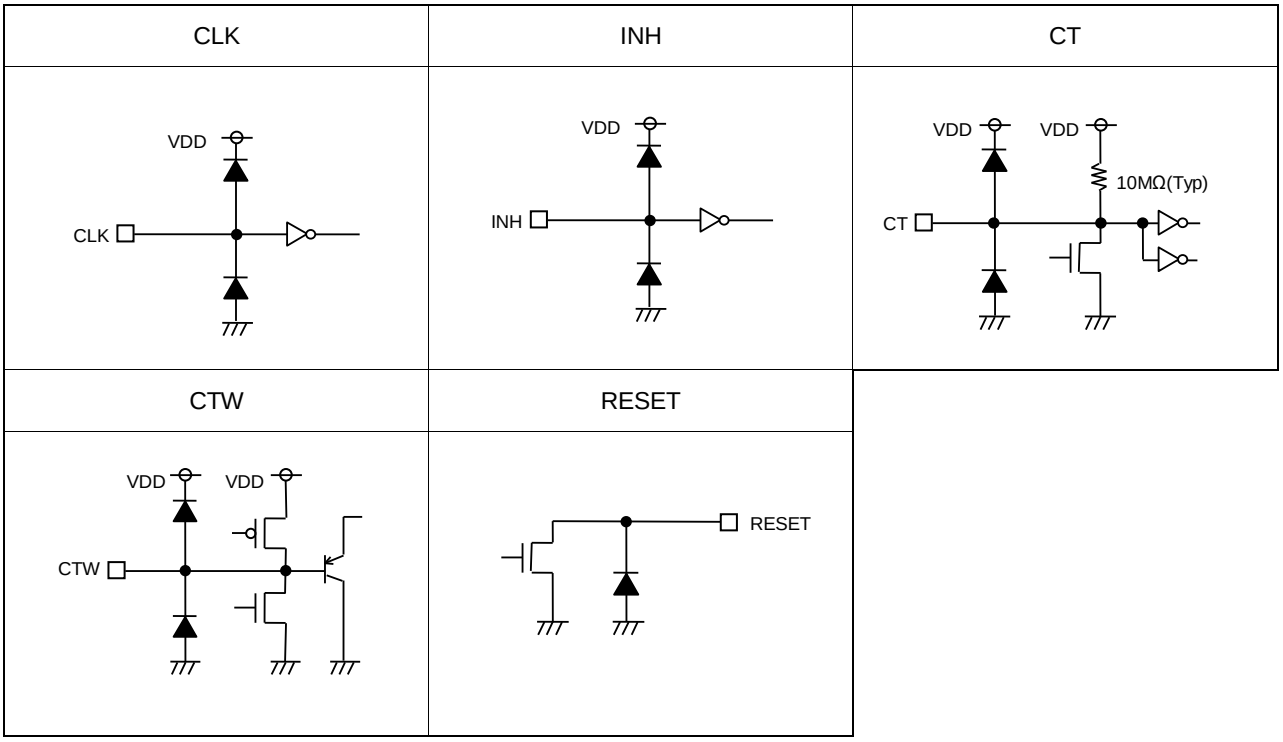


Figure 17. I/O equivalence circuit

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External Settings for Pins and Precautions

1. Connect a capacitor (0.001 µF to 1,000 µF) between the VDD and GND pins when the power line impedance is high. Use of the IC when the power line impedance is high may result in oscillation.

2. External capacitance
A capacitor must be connected to the CTW pin. When using a large capacitor such as 1 µF, the INH pin must allow a CTW discharge time of at least 2 ms. The power-on reset (RESET Transmission Delay) time is given by equation [1] on page 8. The WDT time is given by equations [2] and [3] on page 8. The setting times are proportional to the capacitance value from the equations, so the maximum and minimum setting times can be calculated from the electrical characteristics according to the capacitance. Note however that the electrical characteristics do not include the external capacitor's temperature characteristics.

Operational Notes

1. Reverse Connection of Power Supply
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

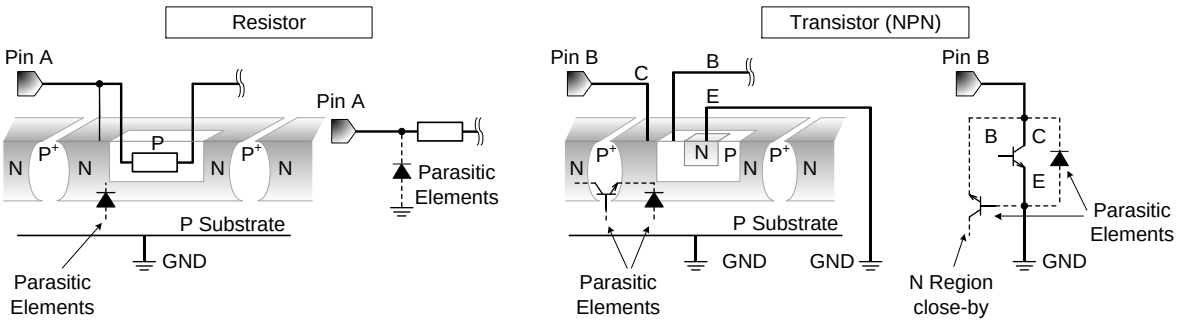


Figure 18. Example of monolithic IC structure

12. Applications or inspection processes with modes where the potentials of the VDD pin and other pins may be reversed from their normal states may cause damage to the IC's internal circuitry or elements. Use an output pin capacitance of 1000 µF or lower in case VDD is shorted with the GND pin while the external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with VDD or bypass diodes between VDD and each pin.

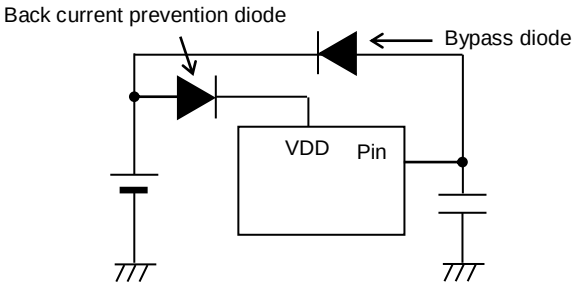


Figure 19.

13. When VDD falls below the operating marginal voltage, output will be open. When output is being pulled up to input, output will be equivalent to VDD.

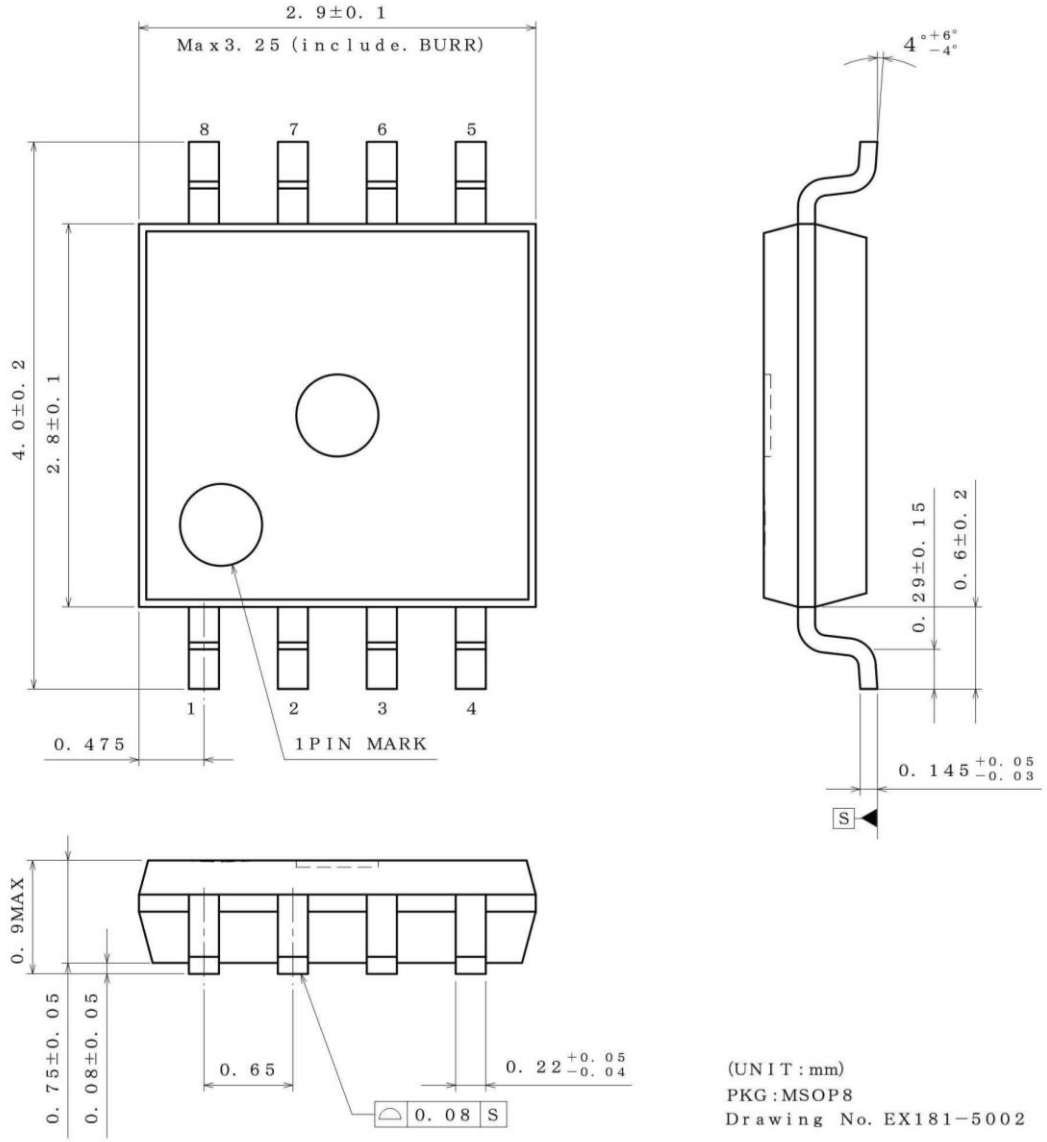
14. Regarding the CLK and INH pins

The CLK and INH pins comprise inverter gates and should not be left open. (These pins should be either pulled up or down.) Input to the CLK pin is detected using a positive edge trigger and does not affect the CLK signal duty. Input the trigger to the CLK pin within the t_{WH} time.

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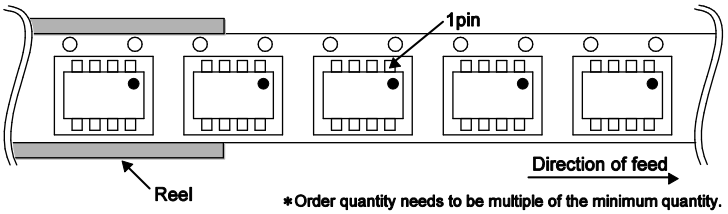
Physical Dimension, Tape and Reel Information

Package Name	MSOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)

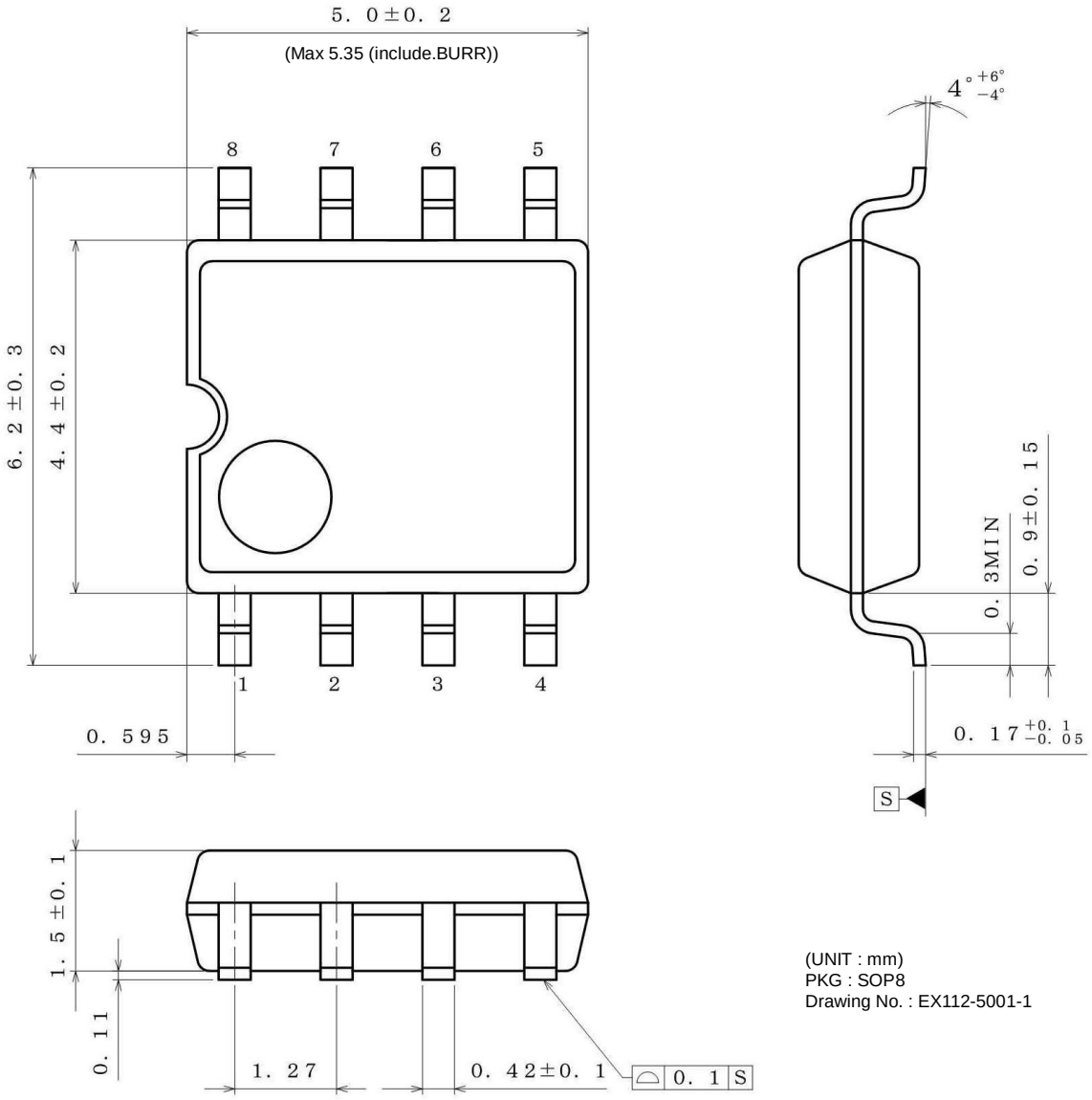


*Order quantity needs to be multiple of the minimum quantity.

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Physical Dimension, Tape and Reel Information – continued

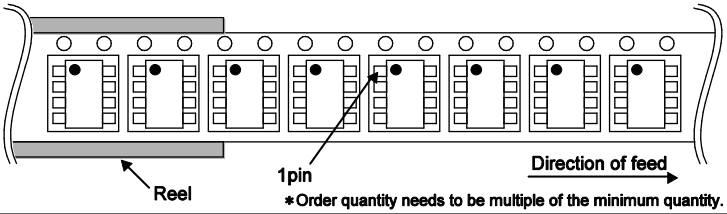
Package Name	SOP8



(UNIT : mm)
PKG : SOP8
Drawing No. : EX112-5001-1

<Tape and Reel information>

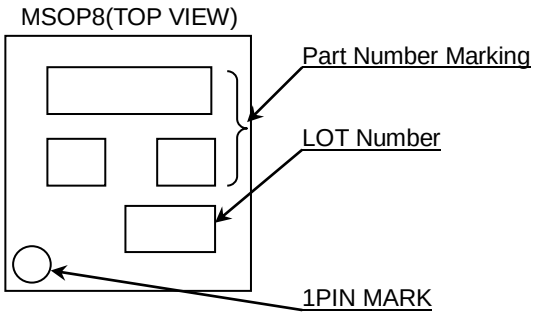
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

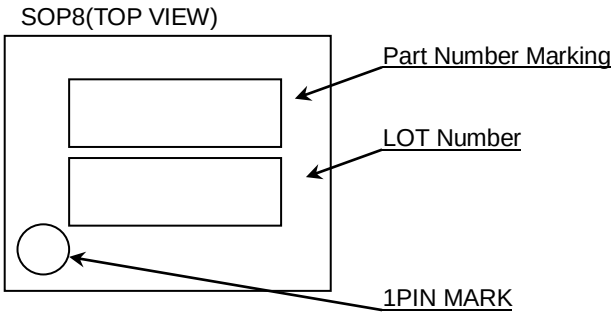


*Order quantity needs to be multiple of the minimum quantity.

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Marking Diagrams





Part Number Marking	Package		Part Number
D3719	MSOP8	Reel of 3000	BD37A19FVM-TR
D3741	MSOP8	Reel of 3000	BD37A41FVM-TR
D8728	MSOP8	Reel of 3000	BD87A28FVM-TR
D8729	MSOP8	Reel of 3000	BD87A29FVM-TR
D8734	MSOP8	Reel of 3000	BD87A34FVM-TR
D8741	MSOP8	Reel of 3000	BD87A41FVM-TR
99A41	SOP8	Reel of 2500	BD99A41F-E2

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Revision History

Date	Revision	Changes
12.Apr.2013	001	New Release
25.Apr.2013	002	P.8 Explanation ⑨ modified. P.9 Figure 17. I/O equivalence circuit the error in writing of the part of CLK was corrected.
05.Sep.2014	003	Applied the ROHM Standard Style
05.Jul.2018	004	P.6 Unit of Figure 9. modified. P.8 Explanation ②, ④ and ⑤ added unit. Explanation ⑥ added number of the expression. P.9 I/O Equivalence Circuit modified. P.10 External Settings for Pins and Precautions 2. modified.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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